

Compal Confidential

Skylake-U M/B Schematics Document

Intel ULV Processor with LPDDR3

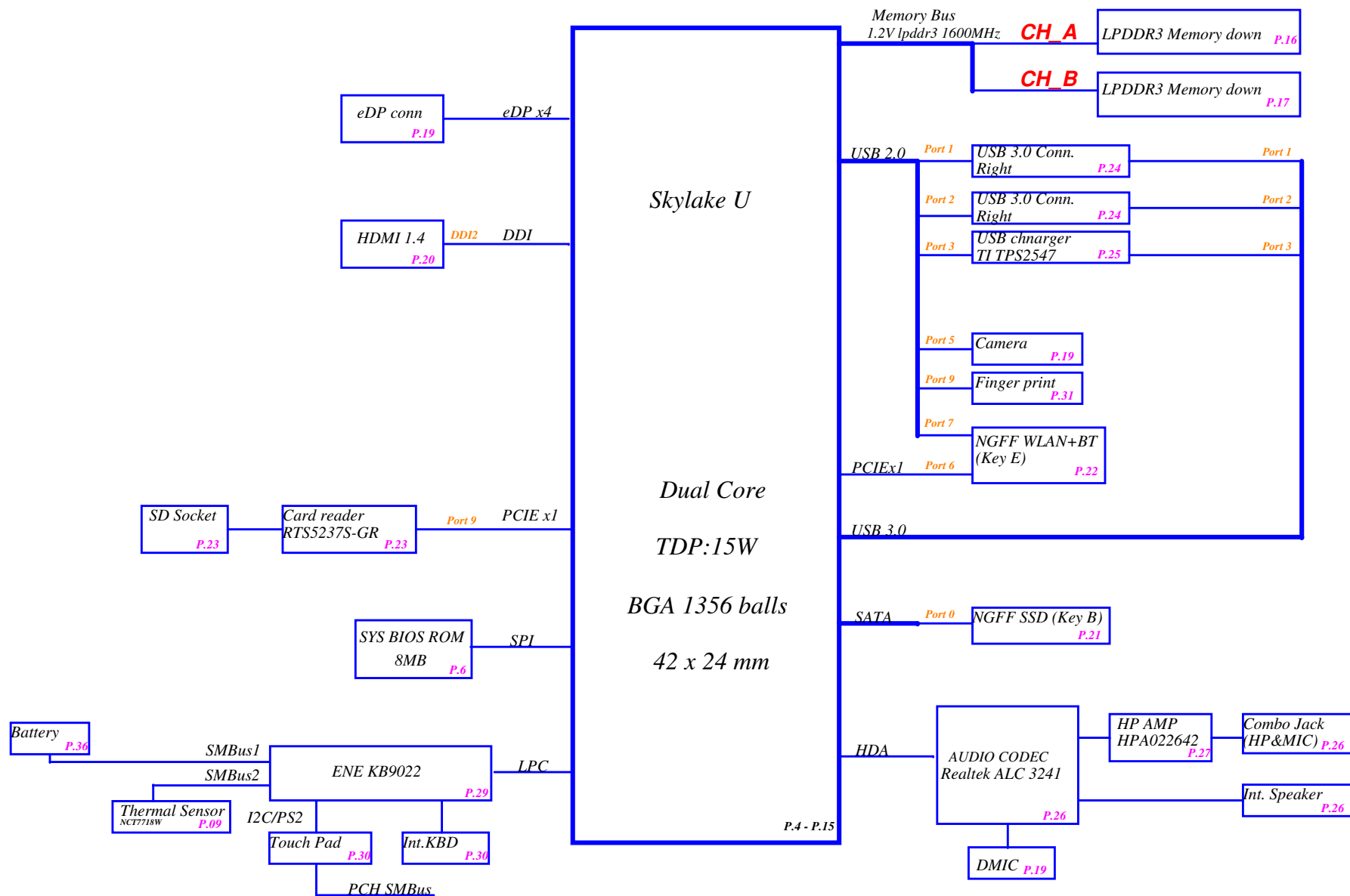
Date : 2015/05/28

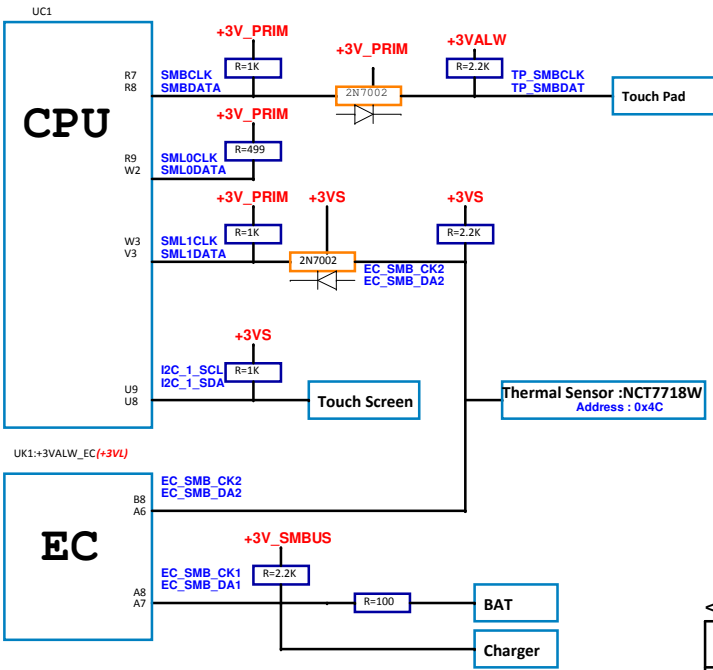
Version 0.3

*Project : Valrhona (13")
ASE30 : LA-C482P*

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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title Cover Page		
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Skylake U Block Diagram





SOC SMBUS Address Table

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SMBCLK SMBDATA	+3VS_PRIM (+3VS)	Touch PAD	TBC	TBC	TBC
SML0CLK SML0DATA	+3V_PRIM				
SML1CLK SML1DATA	+3VS_PRIM (+3VS)	EC	EC define	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VL_EC	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SMB_CK2 EC_SMB_DA2	+3VS	Thermal Sensor	0x4C	0x98	0x99
		PCH	TBC	TBC	TBC

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0					
I2C 1	+3VS	Touch Panel	TBC	TBC	TBC

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

<PCI-E,SATA,USB3.0>

Lane#	PCI-E	SATA	USB3.0	DESTINATION	USB2.0	DESTINATION
1			1	USB3.0	1	USB 2.0/3.0
2			2	USB3.0	2	USB 2.0/3.0
3			3	USB3.0	3	USB 2/3 (Charger)
4			4		4	X
5	1		5	GPU(DIS only) 13" NO USED	5	Camera
6	2		6		6	X
7	3				7	WLAN/BT
8	4				8	Touch screen(Options)
9	5				9	FingerPrint
10	6			WLAN	10	X
11	7	0		SSD		
12	8	1				
13	9			CardReader		
14	10					
15	11	1*				
16	12	2				

<USB2.0 port>

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+12.6VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+1.0V_PRIM	System +1.0V power rail	ON	ON	ON	ON*	OFF
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	+1.2V power rail CPU&LPDDR3	ON	ON	ON	OFF	ON
+1.8V_MEM	+1.8V power rail for LPDDR3	ON	ON	ON	OFF	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VLP	+12.6VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

BOM Structure Table

Function	Stuff	Un-Stuff
NC Components		@
EMI Components	EMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
ME Cnector	CONN@	@CONN@
SPI_IO3(MOW36)	ES@	
TPM	TPM@	

CPU Memory down vender control table

CPU_GPP_G1	CPU_GPP_G2	CPU_GPP_G3	CPU_GPP_G4	Vender	MD size	Vender description	Note	Project
SDRAM_ID4	SDRAM_ID3	SDRAM_ID2	SDRAM_ID1					
0	0	0	0	X	X	X	SODIMMx2 (A,B)	15"/17"
0	0	0	1	X	X	X	SODIMMx1(A) No MDx16bitx4pcs (B)	13"
0	0	1	0	Micron	256x16	MT41K512M16TNA-125-E	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	0	1	1	Samsung	256x16	48BG1646Q-MWK0	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	0	Hynix	256x16	H5TC6G63AMR-PBA	SODIMMx1(A) MDx16bitx4pcs (B)	13"
0	1	0	1	Micron	512x8	MT41K512M8RG-107-N	MDx8bitx8pcs (A)	14"
0	1	1	0	Samsung	512x8	K4B4G0846Q-HYK0	MDx8bitx8pcs (A)	14"
0	1	1	1	Hynix	512x8	H5TC4G83BFR-PBA	MDx8bitx8pcs (A)	14"
1	0	0	0	Elpida	512x8	MT41K512M8RH-125-E	MDx8bitx8pcs (A)	14"
1	0	0	1	Hynix	128Mx32x2	H9CCNNN8GTMLAR-NUD	A - LPDDR3 MDx32bitx2pcs B - LPDDR3 MDx32bitx2pcs	13"
1	0	1	0	Samsung	MD 4G	K4E8E304EE-EGCE		
1	0	1	1	Elpida		EDF8132A3MA-GD-F		
1	1	0	1	Hynix	256Mx16x4	H9CCNNNBJTMLAR-NUD		
1	1	1	0	Samsung	MD 8G	K4E6E304EE-EGCE		
1	1	1	1	Elpida		EDFA232A2MA-GD-F		

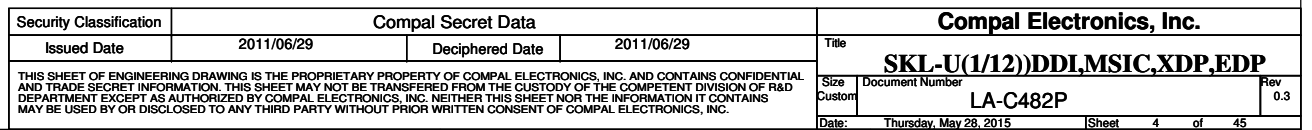
CPU Project ID control table

CPU_GPP_G3 PROJECT_ID4	CPU_GPP_G2 PROJECT_ID3	CPU_GPP_G1 PROJECT_ID2	CPU_GPP_G0 PROJECT_ID1	Project name
SKL-U 0	UMA 0	0	0	13" (Valrhona)
SKL-H 1	DIS 1	0	1	14" (Lindt)
		1	0	15" (Puccini)
		1	1	17" (Maison)

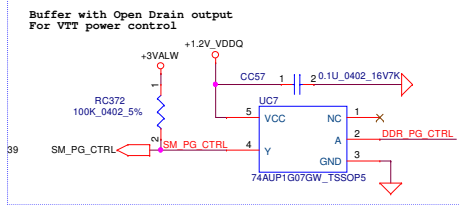
EC Board ID (UMA, Dis, phase) control table

RK13	DB	SI	PV	MV	Note
UMA	0ohm	15Kohm	27Kohm	43Kohm	
Dis	12Kohm	20Kohm	33Kohm	56Kohm	

1 = Port C is detected.

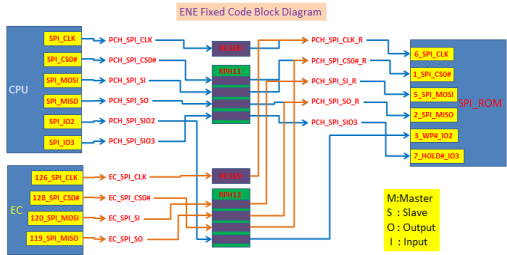
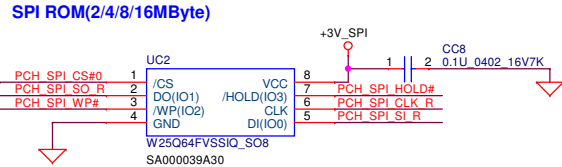
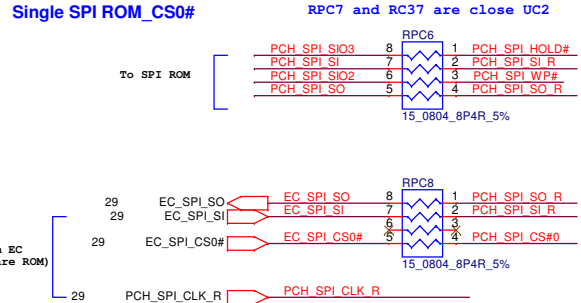
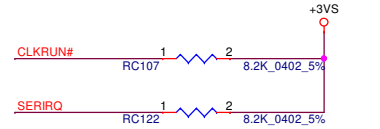
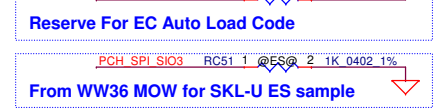
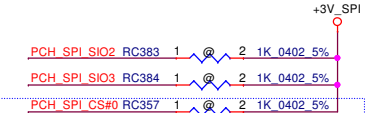
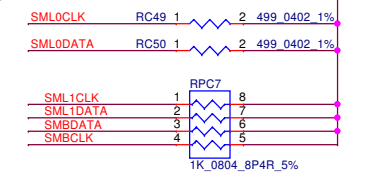
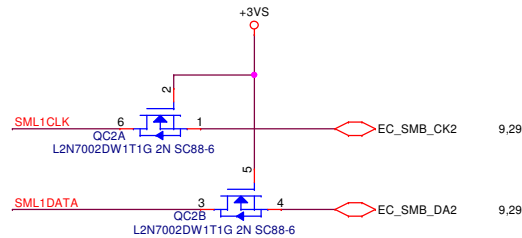
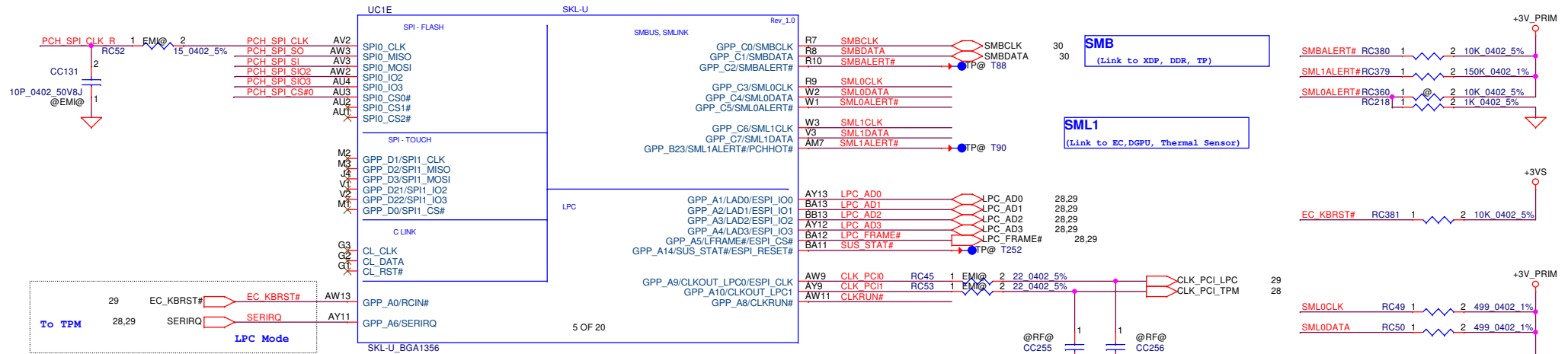


Non-Interleaved



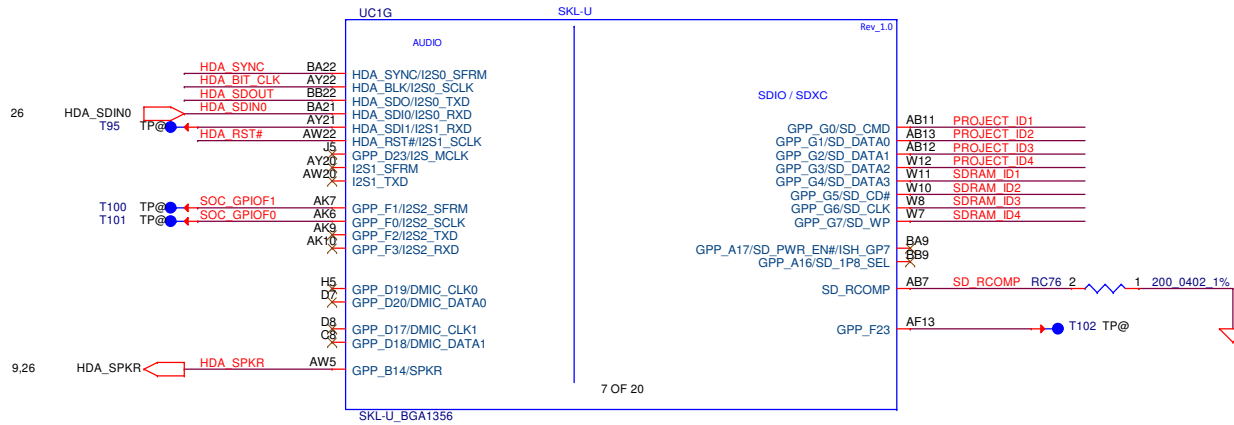
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SML0ALERT# (Internal Pull Down):
eSPI or LPC
0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

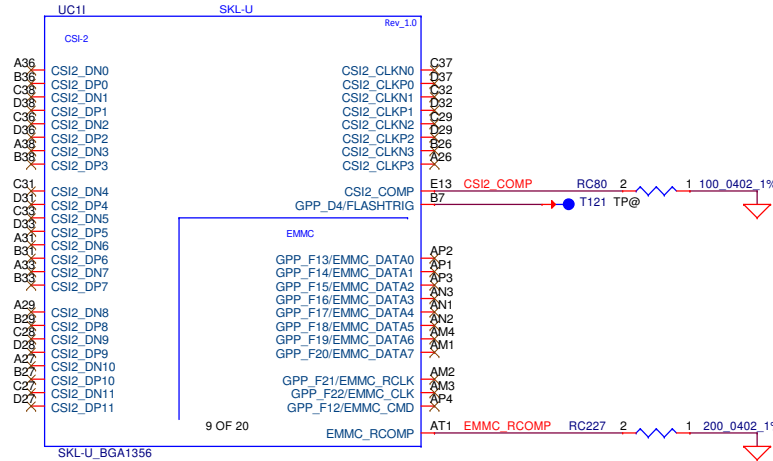
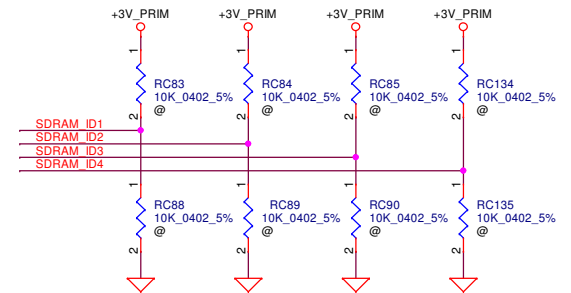
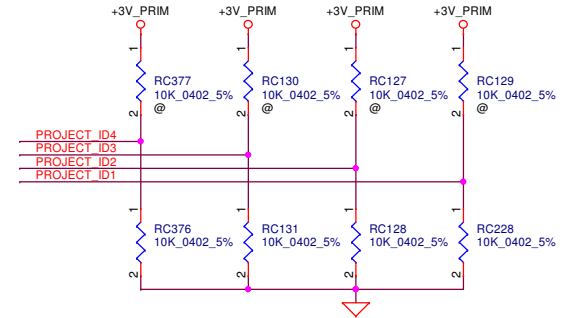
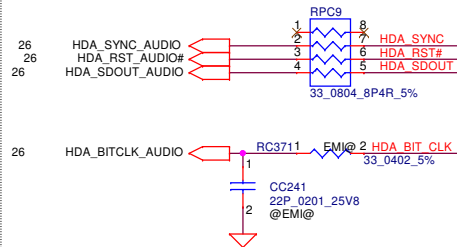


EON	SA000046400	S	IC	FL	64M	EN25Q64-104HIP	SOP	8P
MXIC	SA00006N100	S	IC	FL	64M	MX25L6473EM2I-10G	SOP	8P
WINBOND	SA000039A30	S	IC	FL	64M	W25Q64FVSSIQ	SOIC	8P SPI ROM
Micron	SA00005L100	S	IC	FL	64M	N25Q064A13ESEC0F	SO8W	8P

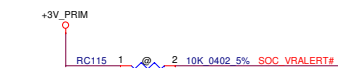
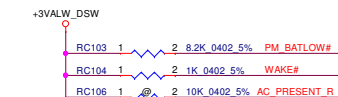
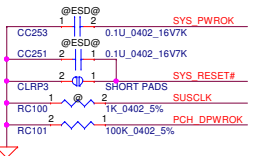
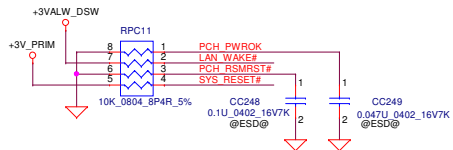
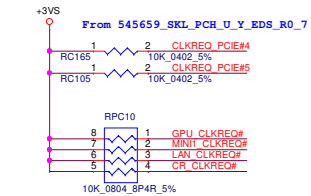
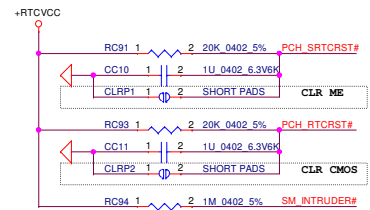
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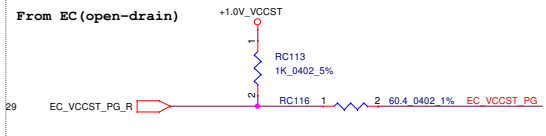
HDA for AUDIO



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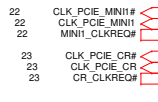


From EC(open-drain)

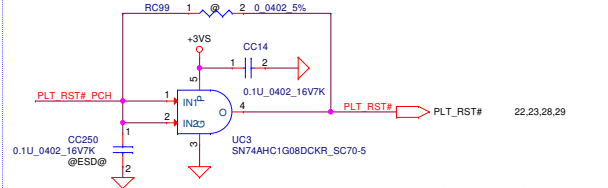


WLAN

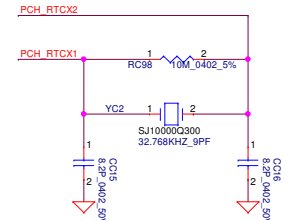
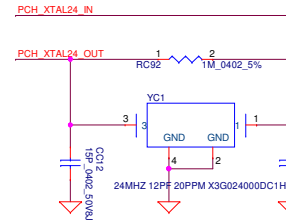
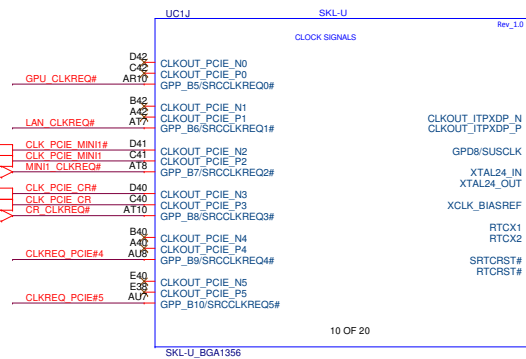
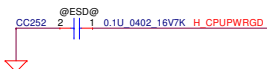
CardReader



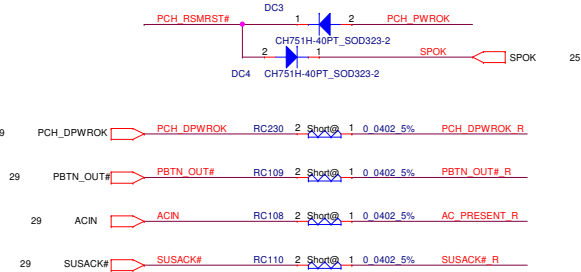
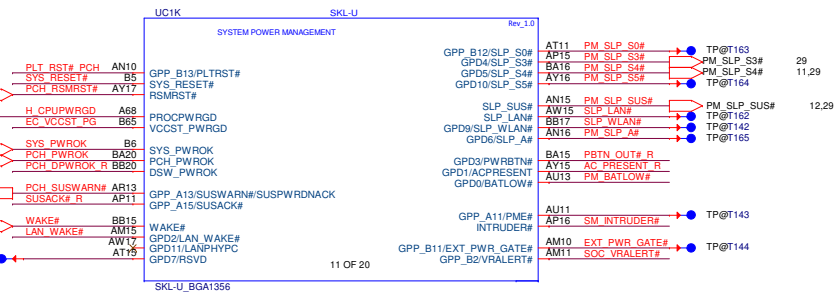
PCH PLTRST Buffer



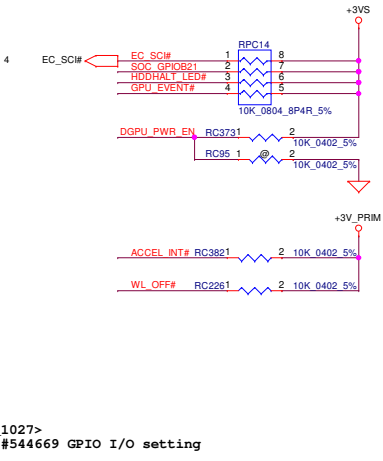
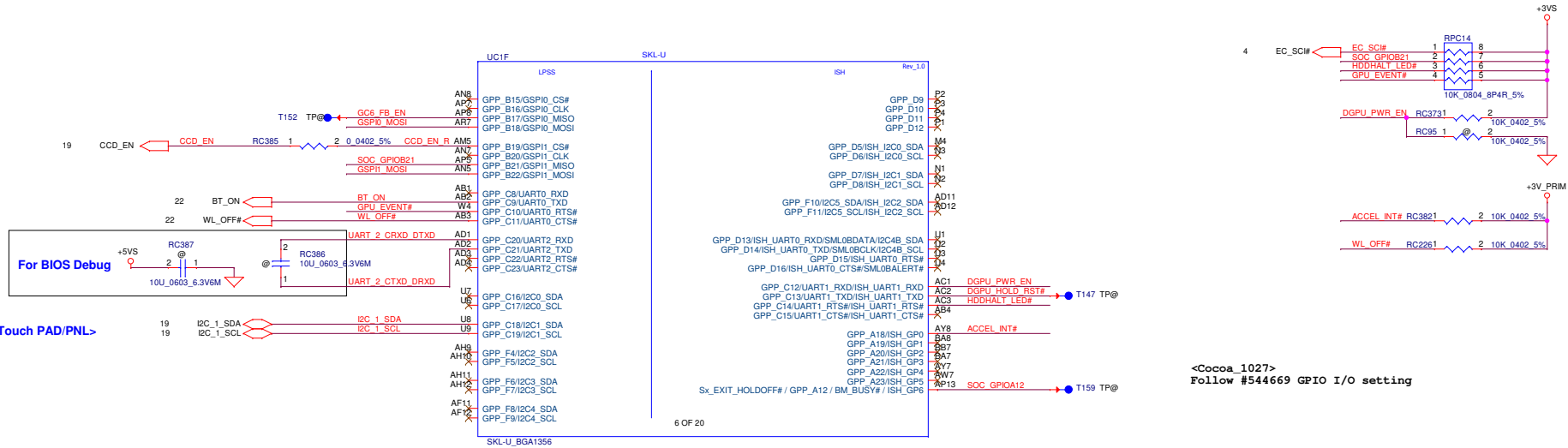
Only For Power Sequence Debug



<Cocoa_1020>
32M use these part (SJ10000NM00, SJ10000MR00) just can meet <50k ohm spec
24M: SJ10000D100, SJ10000CS00



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Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.----> AAX05 Use

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. --> AAX05 Use

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

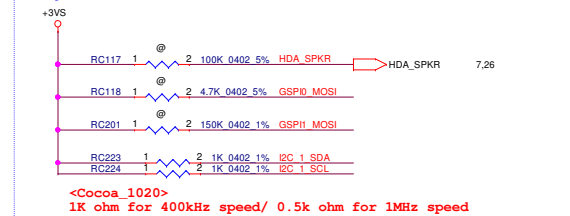
GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

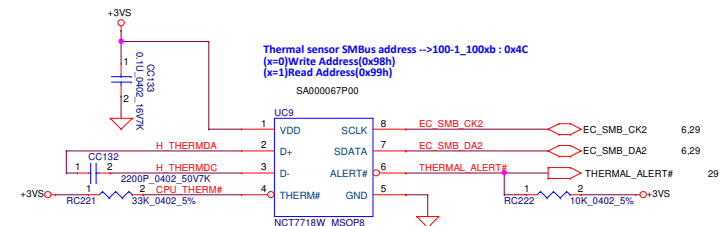
0 = SPI Mode --> AAX05 Use

1 = LPC Mode

Strap Pin



THERMAL SENSOR



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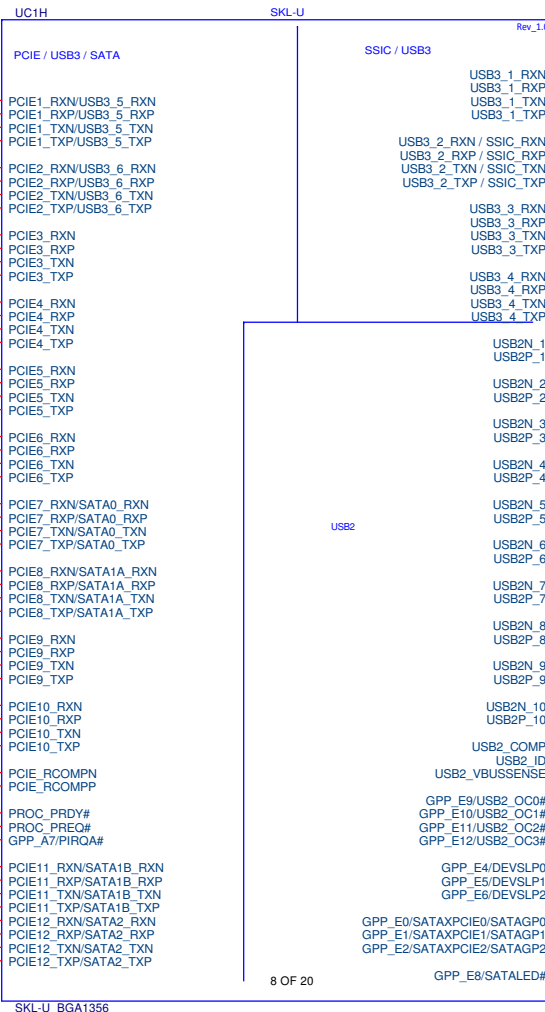
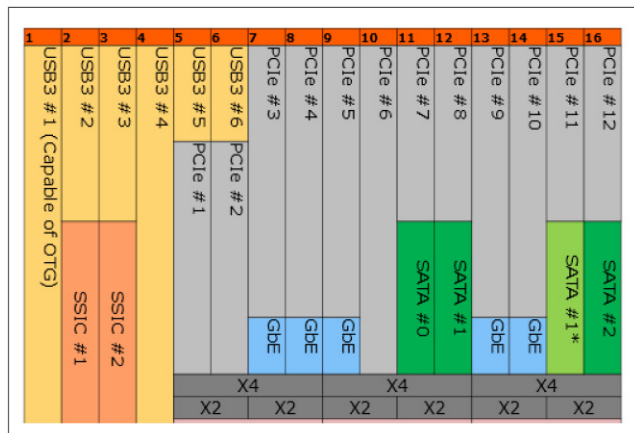
WLAN

SATA SSD

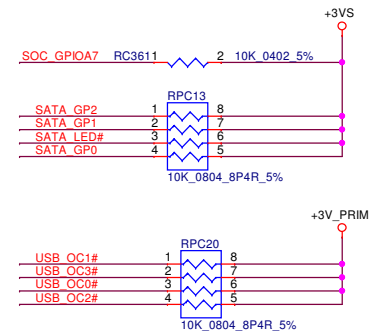
CardReader

When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

High Speed I/O (HSIO) Lane Multiplexing in SKL-U

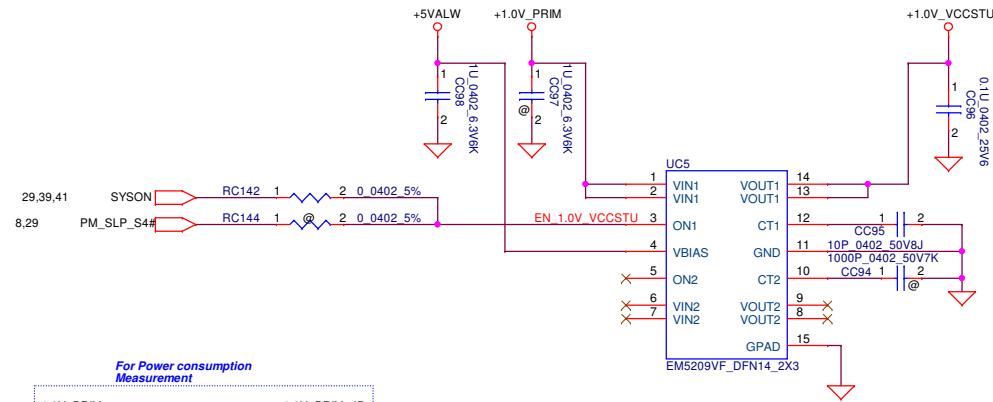


GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1&2
USB_OC1#	USB2 Port 3
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NGFF SSD KEY B
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA



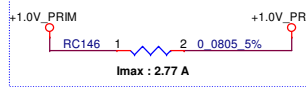
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Size Custom		Document Number		LA-C482P		Rev 0.3					
Date		Thursday, May 28, 2015		Sheet		10		of 45			

+1.0V_PRIM TO +1.0V_VCCSTU

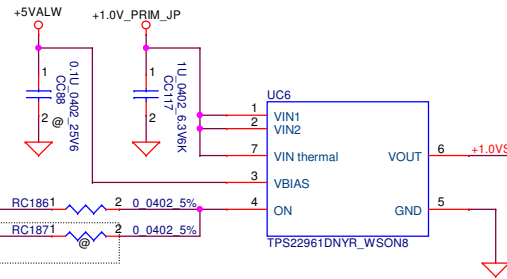


Follow 543977_SKL_PDDG_Rev0_91
CC95 10pF -> 22uS (Spec.<= 65uS)

For Power consumption
Measurement

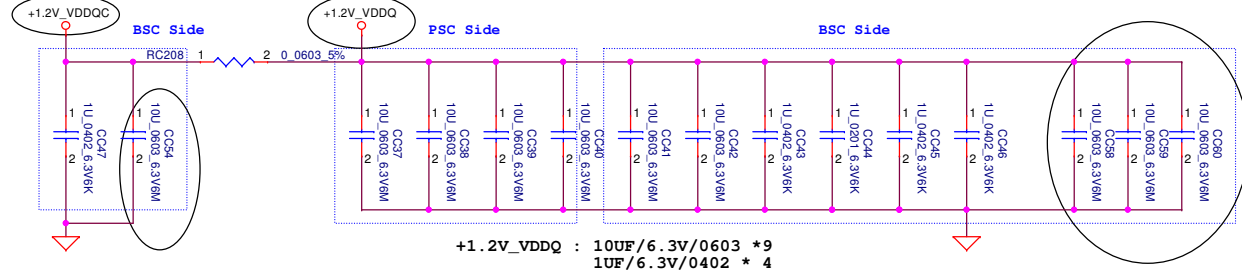
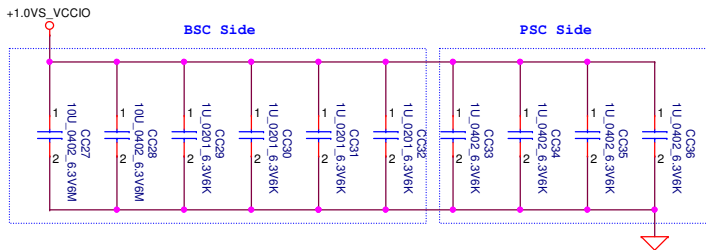


+1.0V_PRIM TO +1.0VS_VCCSTG / +1.0VS_VCCIO

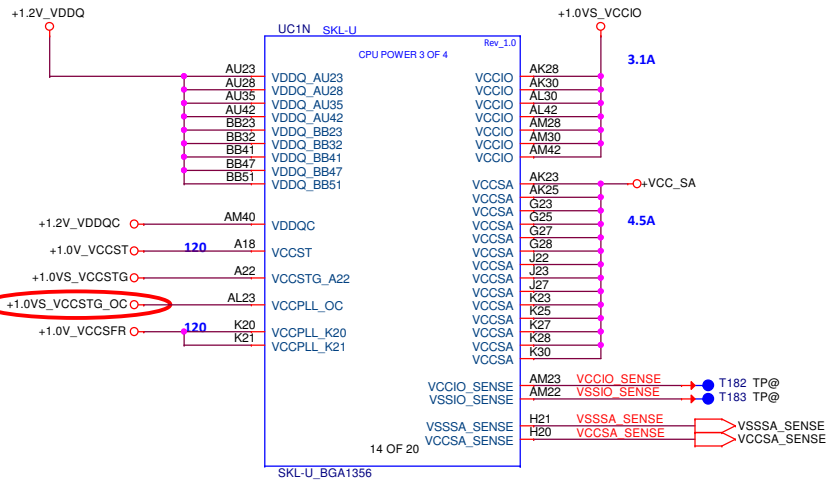


For Verify S0IX

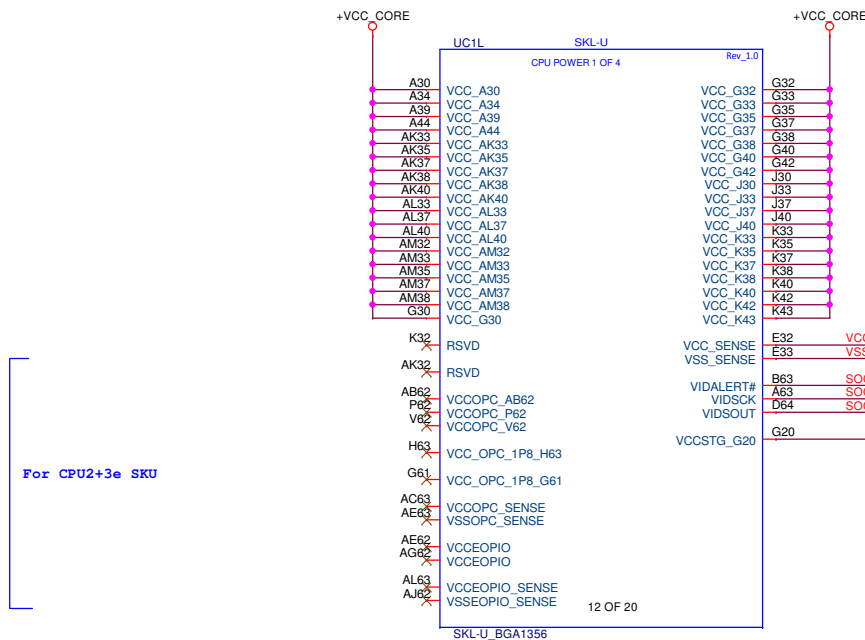
RC208 Follow 544669_SKL_U_DDR3L_RVP7_Schematic_Rev0_53
CC47, CC54 Follow 549914_SKL_U_LPDDR3_RVP5



+1.2V_VDDQ : 10uF/6.3V/0603 *9
1uF/6.3V/0402 * 4



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				Date	Thursday, May 28, 2015
				Sheet	11 of 45



Trace Length < 25 mils

Trace Length < 25 mils

Trace Length < 25 mils

Trace Length < 25 mils

Trace Length < 25 mils

Trace Length < 25 mils

Trace Length < 25 mils

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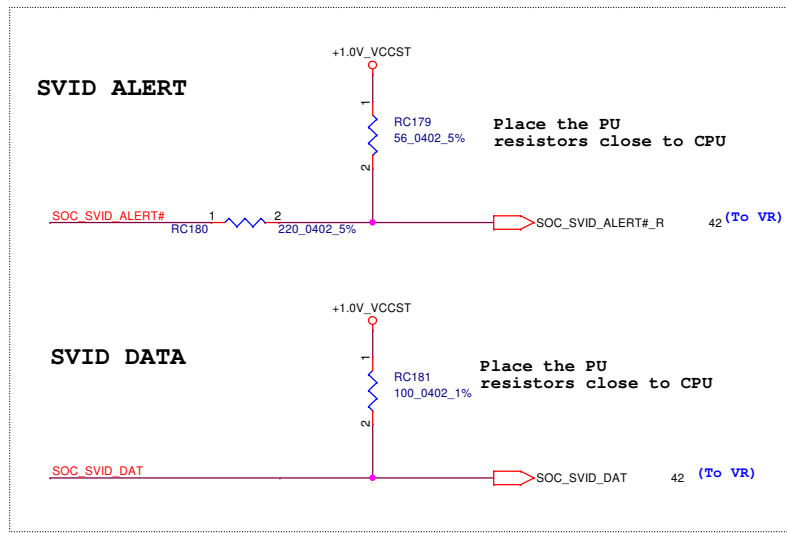
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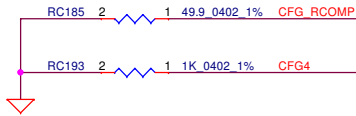
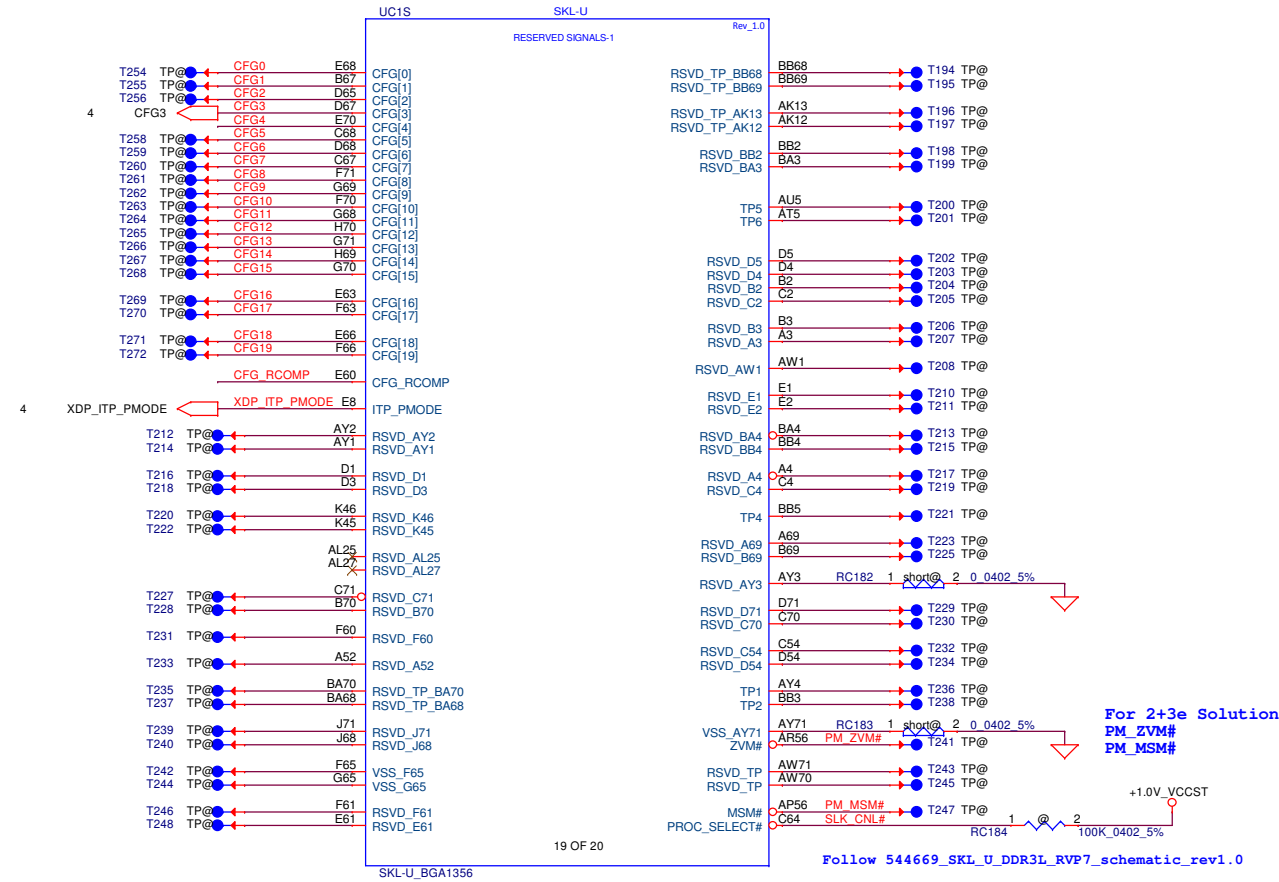
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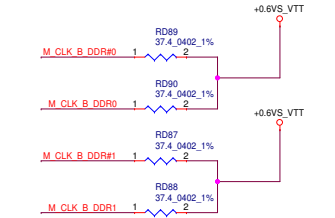
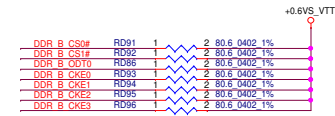
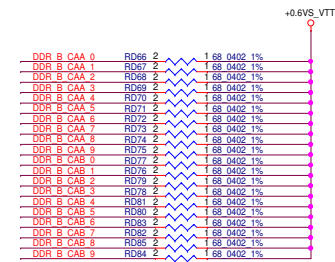
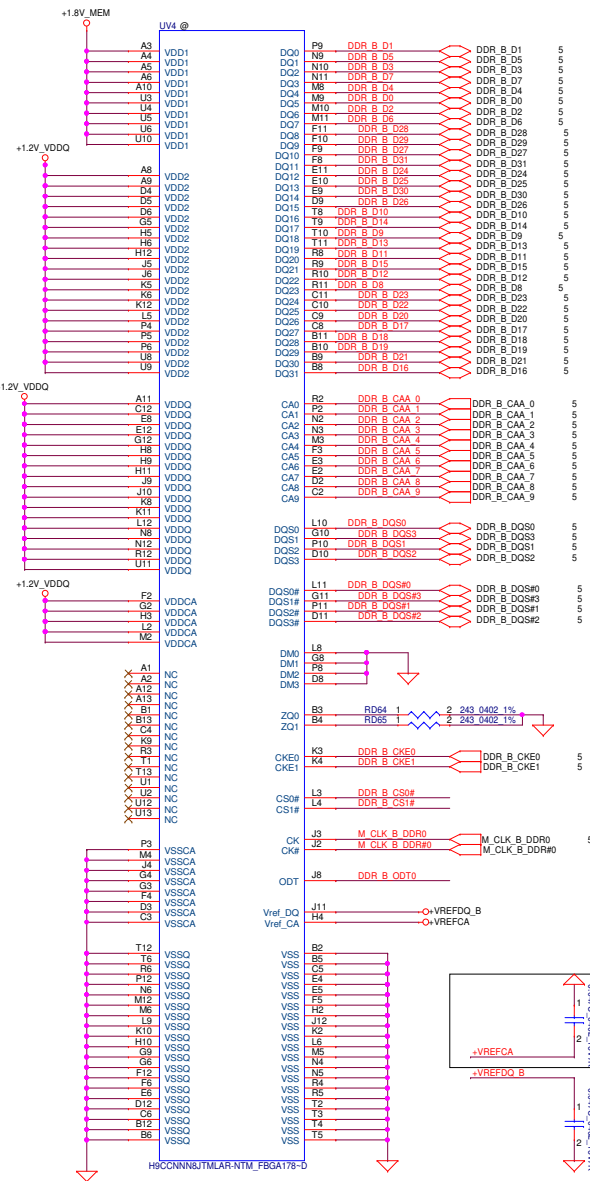
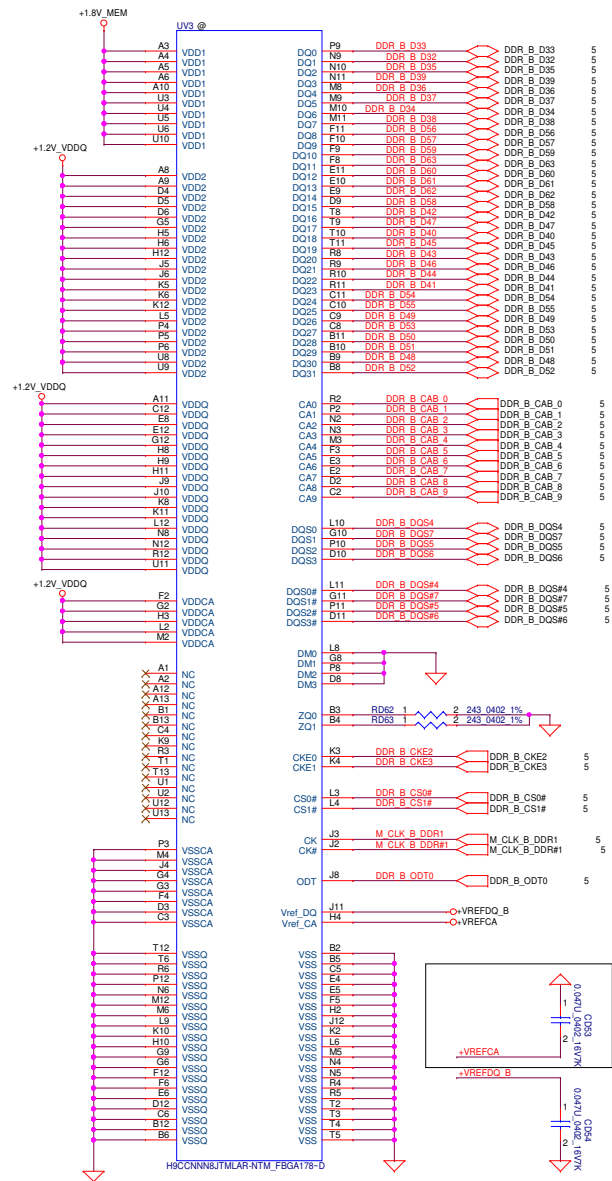
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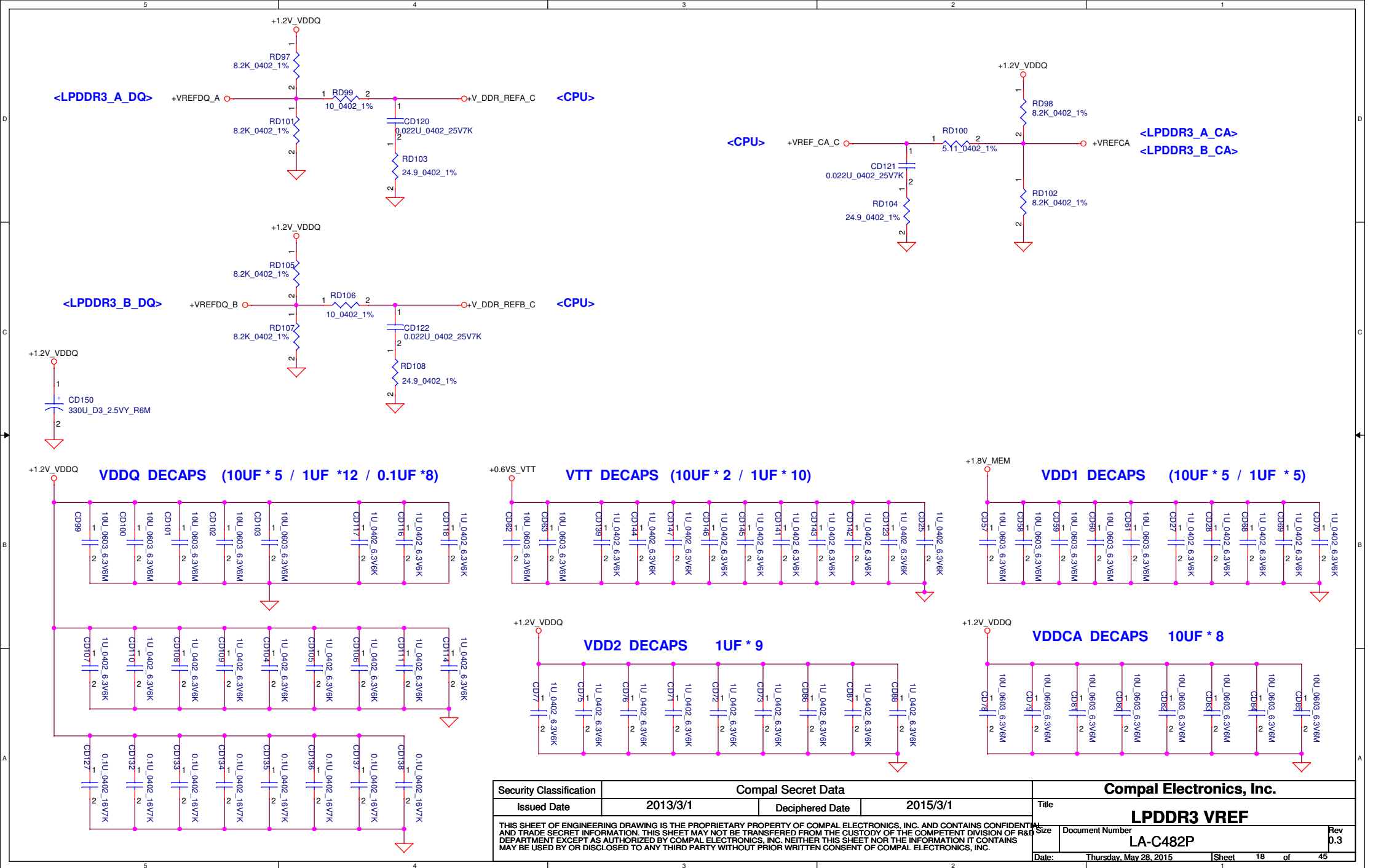
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				LA-C482P	
				Date	Thursday, May 28, 2015
				Sheet	13 of 45

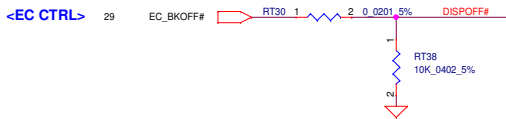
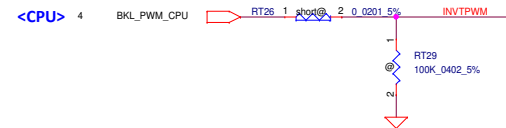
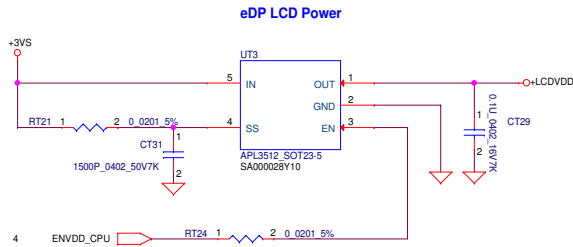


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

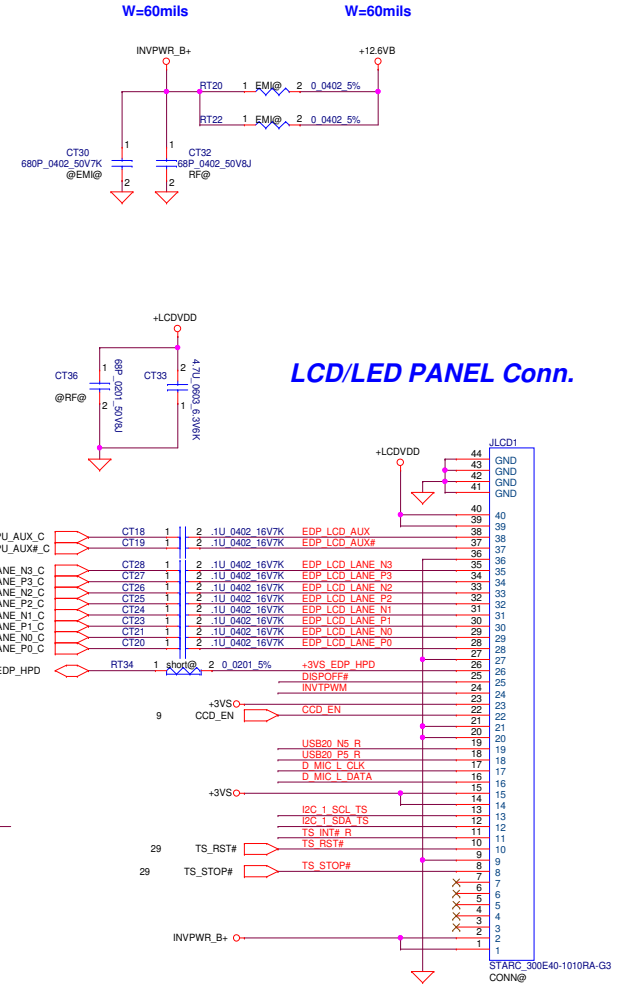
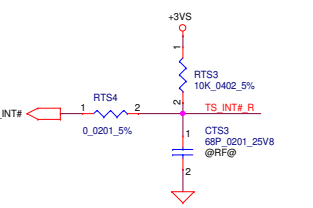
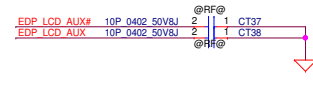
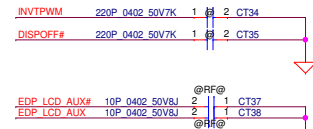
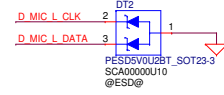
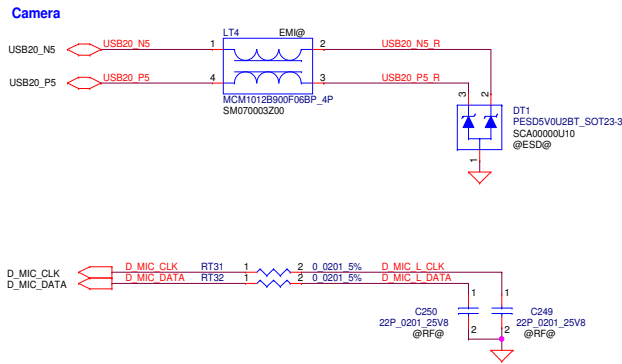
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/05/27	Deciphered Date	2011/05/11	Title	SKL-U(12/12)RSVD
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				Date	Thursday, May 28, 2015
				Sheet	15 of 45
				Rev	0.3





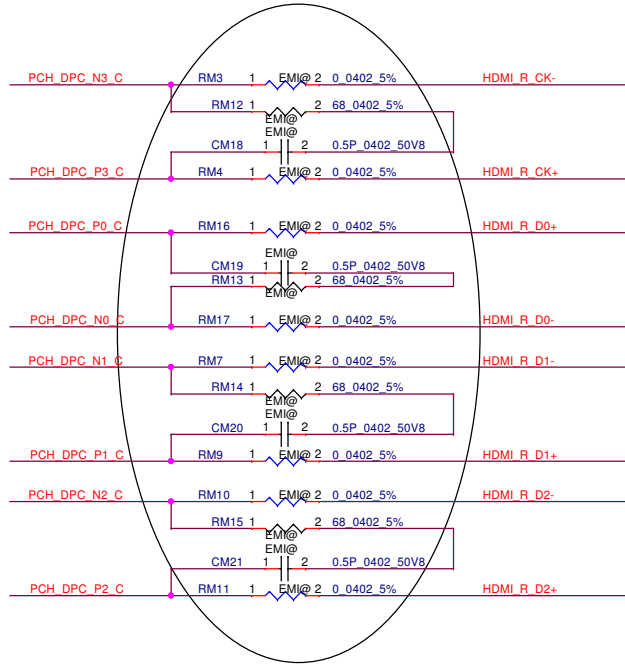
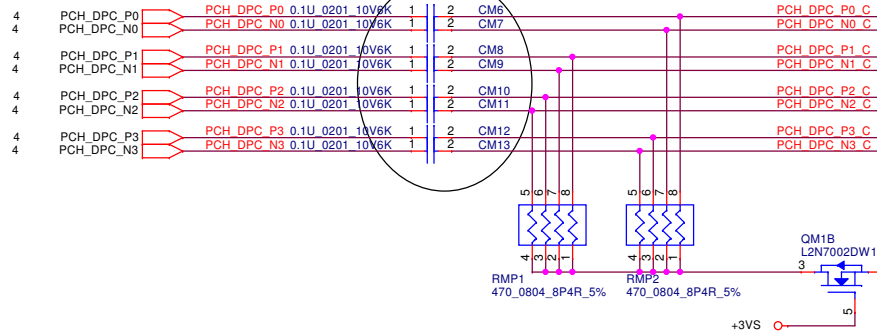


Touch Screen

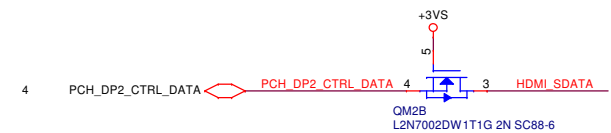
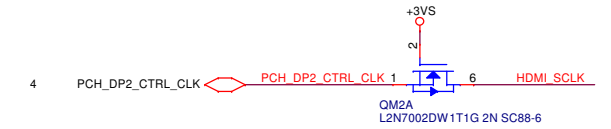
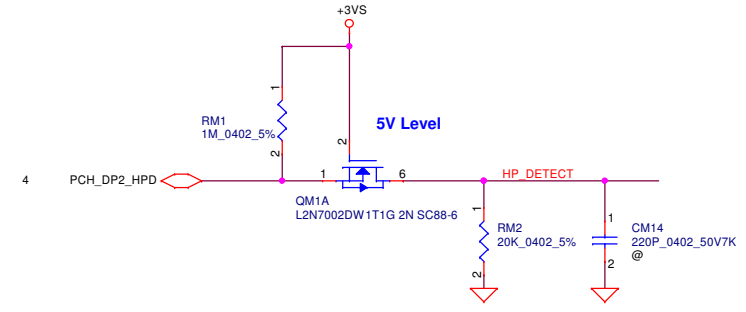
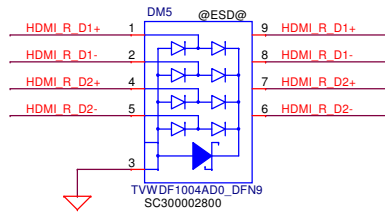
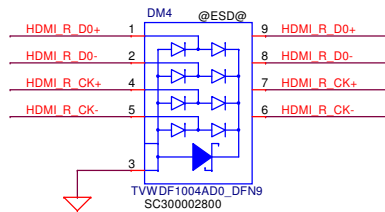
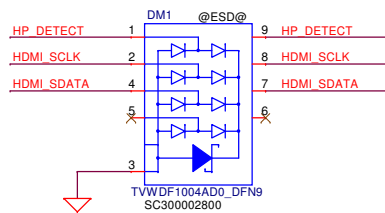
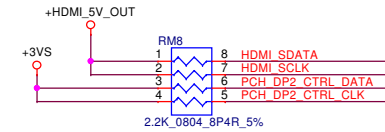
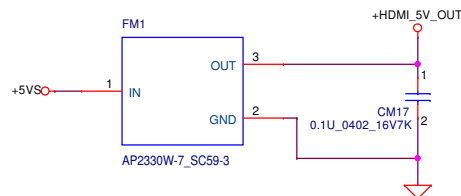


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Size	Document Number	LA-C482P		Rev	0.3
Date:	Thursday, May 28, 2015	Sheet	19	of	45

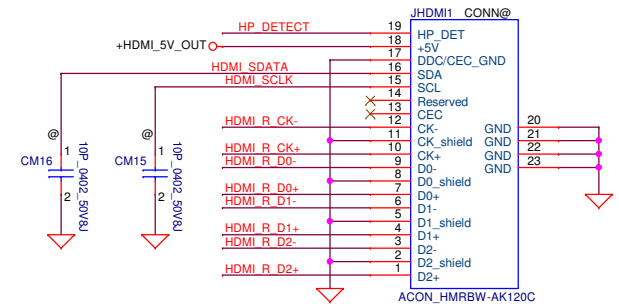
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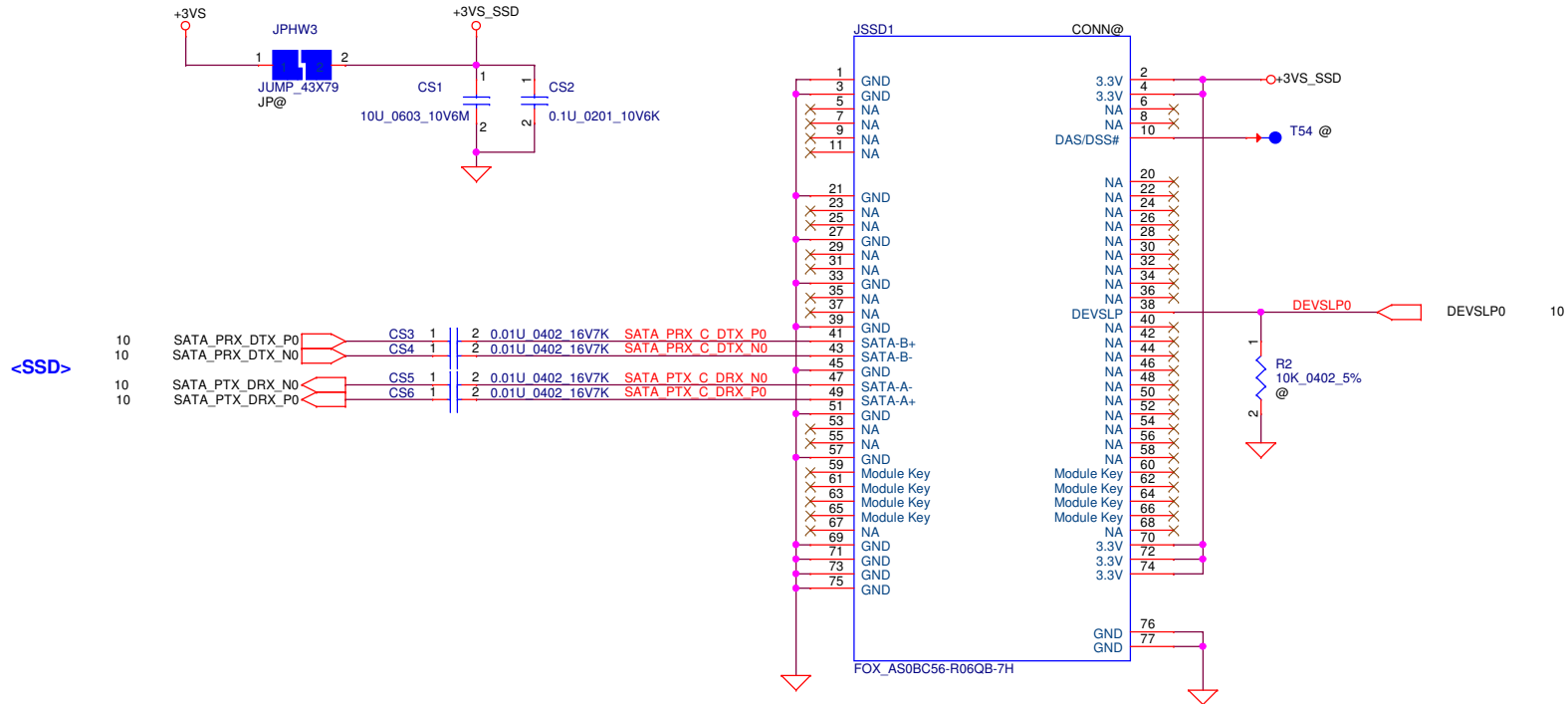


HDMI Conn.



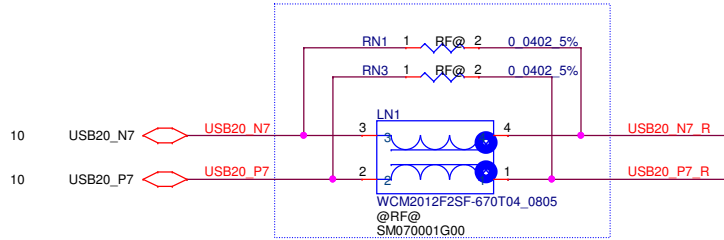
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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Size		Document Number		Rev	
Date		Thursday, May 28, 2015		Sheet 20 of 45	

JPHW3 need to short

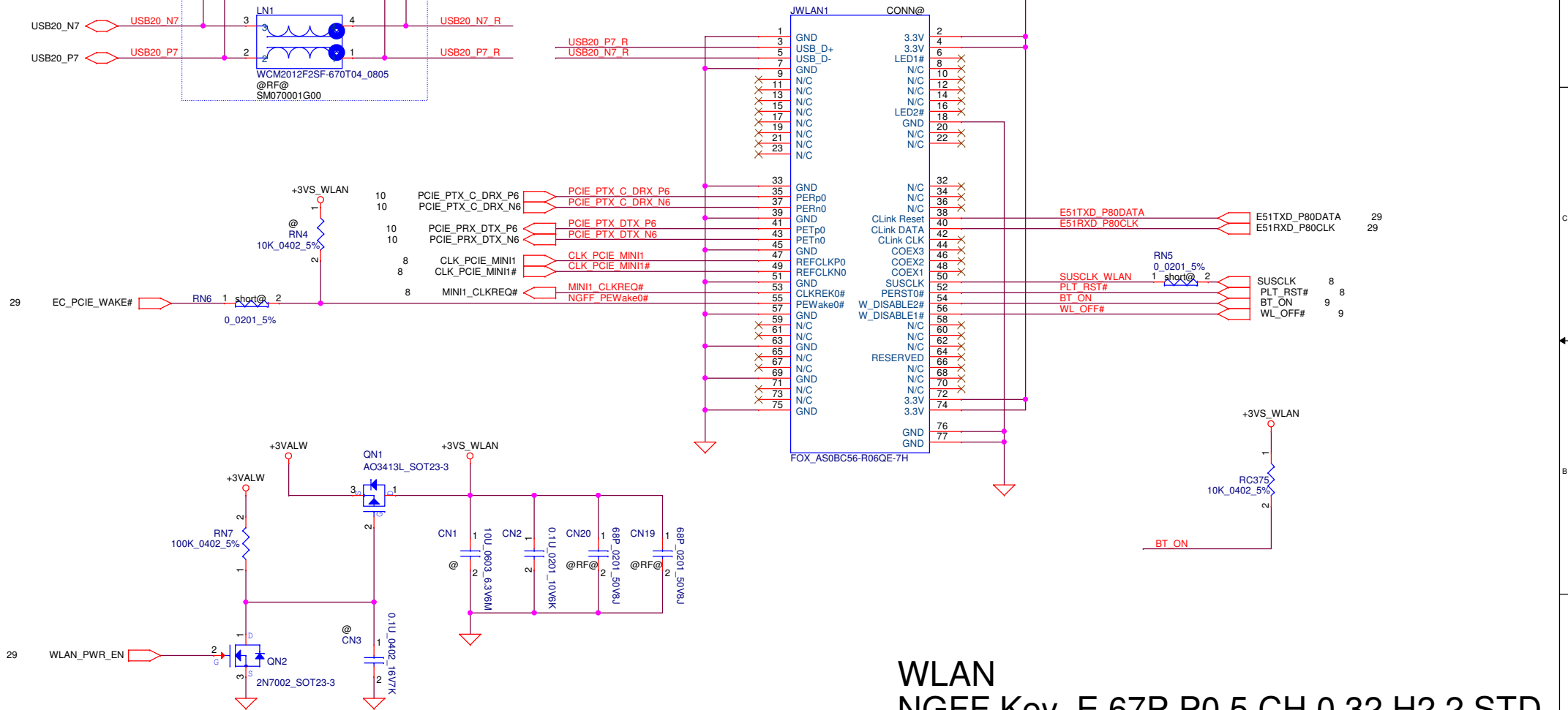


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Size B		Document Number			Rev 0.3
Date:		Thursday, May 28, 2015			Sheet 21 of 45

Co-Lay

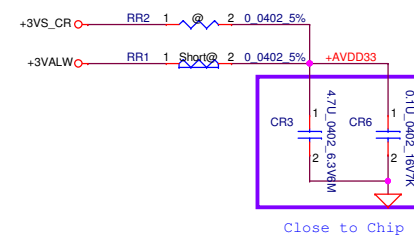
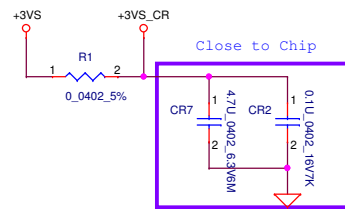
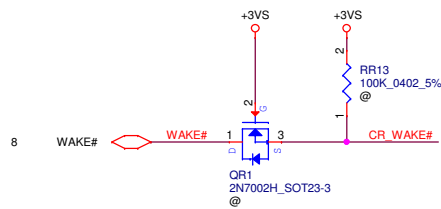


WLAN NGFF

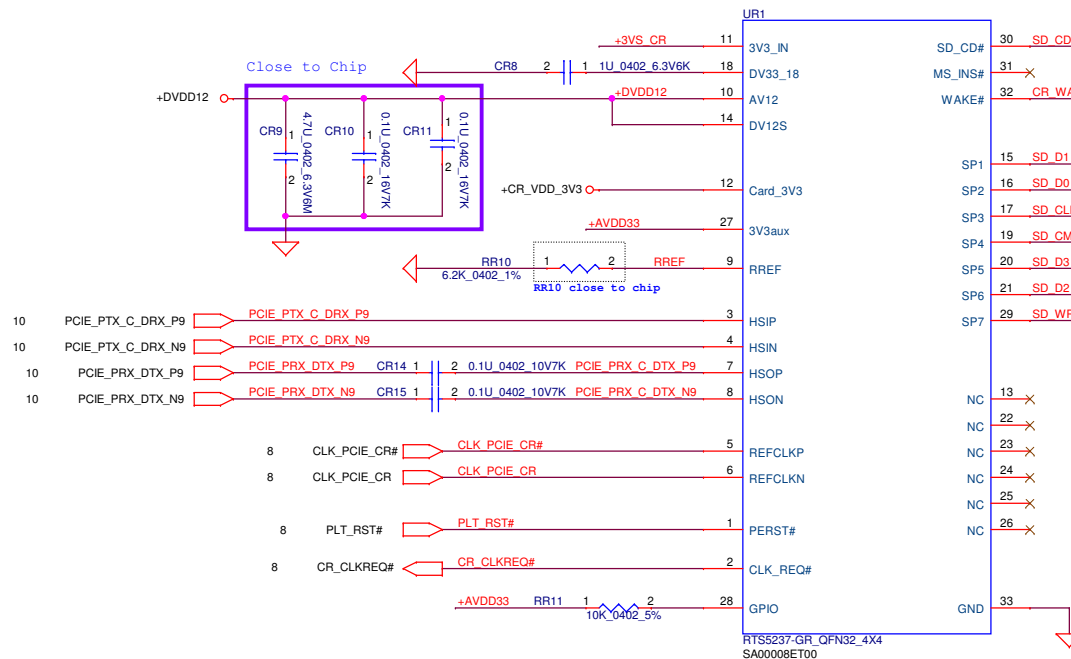


WLAN NGFF Key_E 67P P0.5 CH 0.32 H2.2 STD

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				LA-C482P	



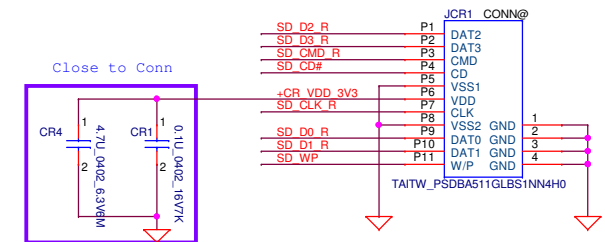
- Complete D3V3 power plane partition under RTS5227 chip and Socket in Power Layer
- Pin 11(3V3_IN) / pin 12 (CARD_3V3) trace width is 40 mils (minimum).
- Pin 27(3V3aux) trace width is 30 mils (minimum).
- Pin 10(AV12), pin 14(DV12S), pin 18 (DV33_18) trace width is 20 mils (minimum).
- Pin 9 (RREF) trace width is 12 mils (minimum).



For pin3 to pin8 :
 1. impedance(Zdiff) is 85±15% (follow Intel)
 2. Maintain at least 20 mils air gap
 3. No more than 5-mil delta between the lengths of the two signals.

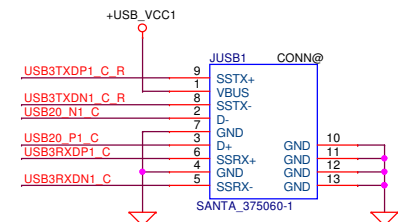
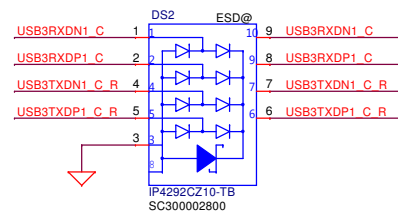
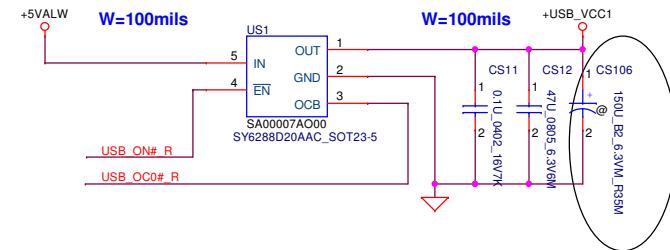
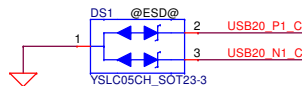
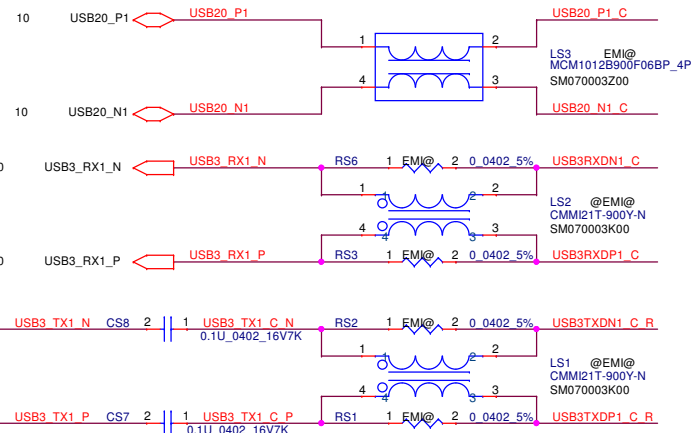
- For pin15 to pin21 :
 ■ CLK ~ DATA | trace length ≤ 100 mils
 ■ DATA.x ~ DATA.y | trace length ≤ 100 mils
 ■ It is recommended that use a guard ground to isolate SD_CLK trace
 ■ These traces of characteristic impedance are 50±15%.

Card Reader Conn

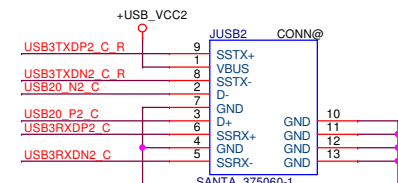
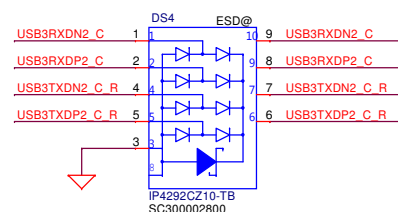
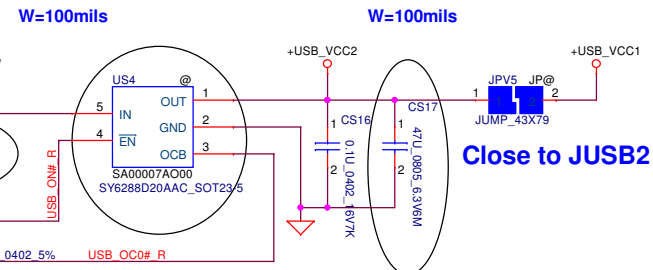
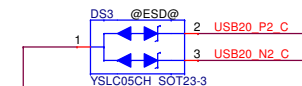
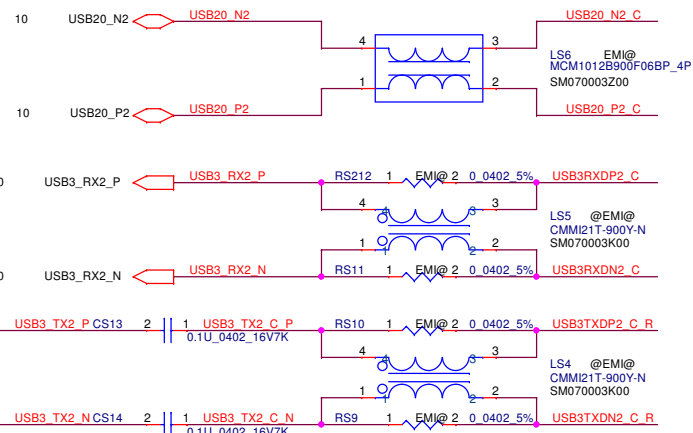


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						Size		Document Number		Rev	
								LA-C482P		0.3	
Date:		Thursday May 28, 2015		Sheet		23 of 45					

USB2.0/USB3.0 port 1

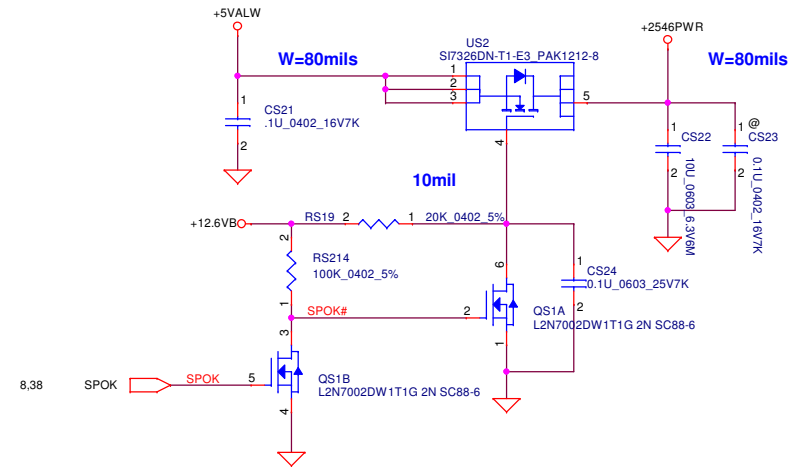
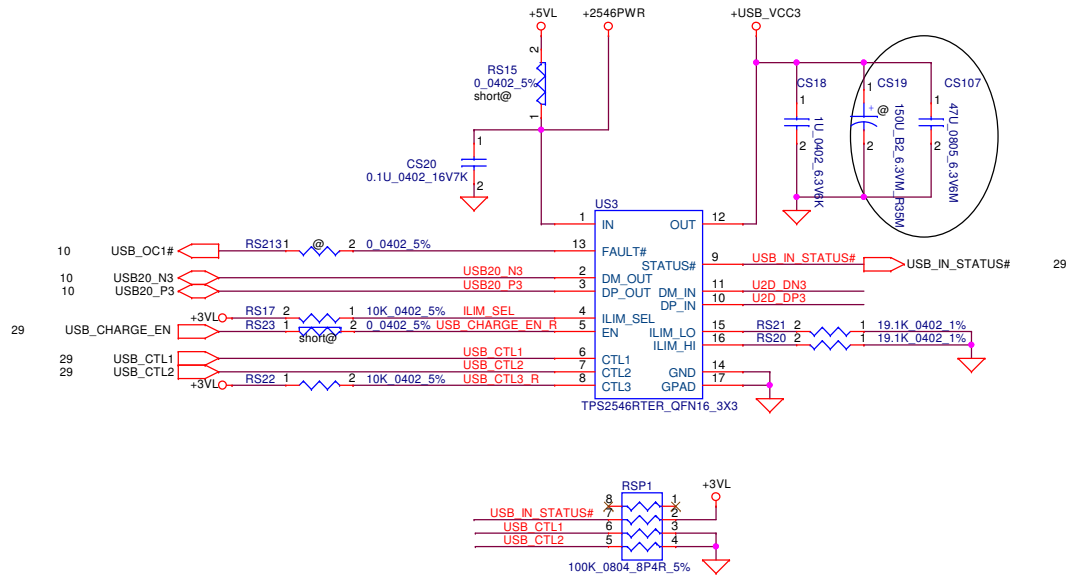


USB2.0/USB3.0 port 2

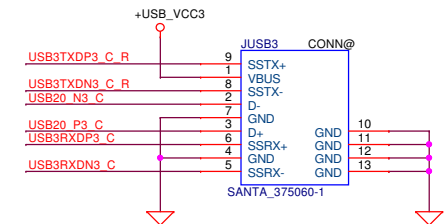
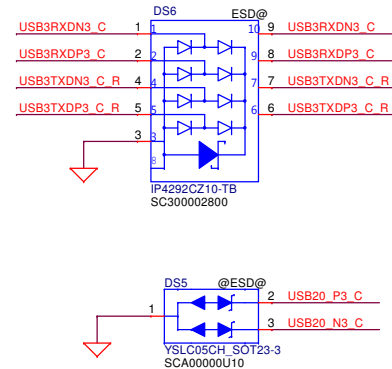
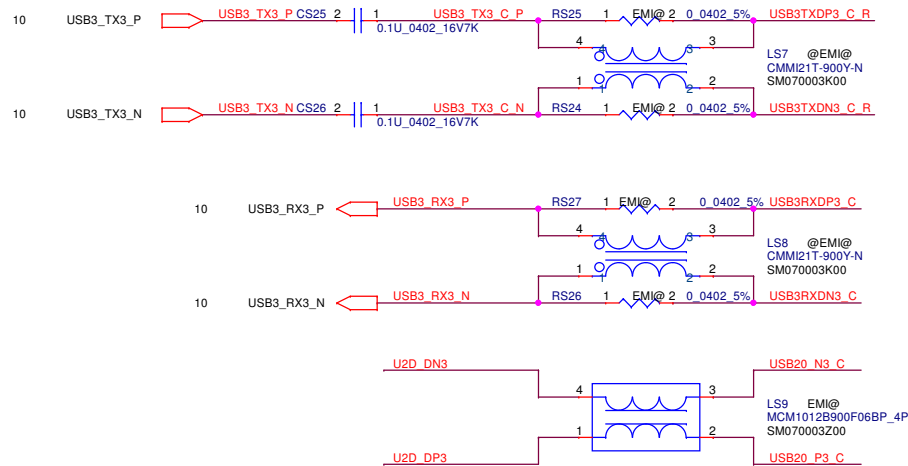


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Size	Document Number	LA-C481P		Rev	0.3
Date:	Thursday, May 28, 2015	Sheet	24	of	45

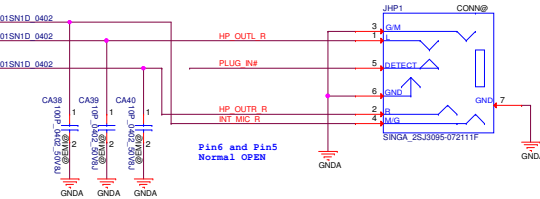
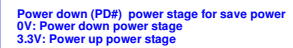
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USB2.0/USB3.0 port 3

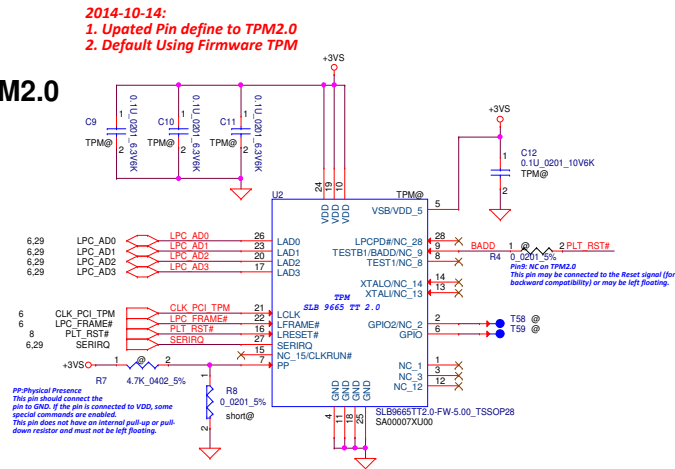


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/04/22	Deciphered Date	2015/04/22	Title USB 3.0/2.0 Charger		
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					LA-C482P	0.3
Date:				Thursday, May 28, 2015	Sheet	25 of 45

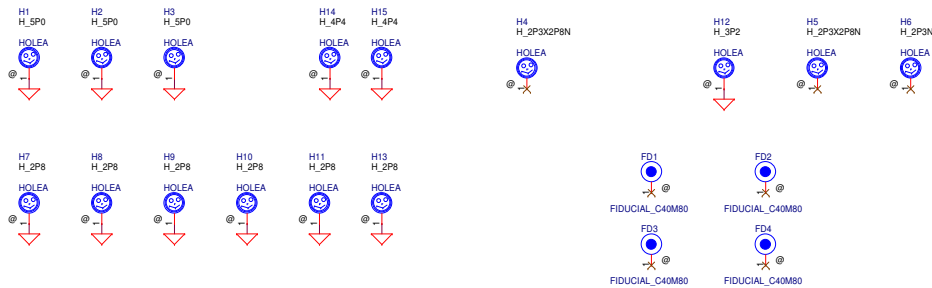


Security Classification	Compel Secret Data		Title		Compel Electronics, Inc.
Issued Date	2013/01/04	Declassified Date	2015/01/04	AUDIO ALC3241-CG	
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				Cushion	0.3
				Date: Thursday, May 28, 2015 Sheet: 25 of 45	

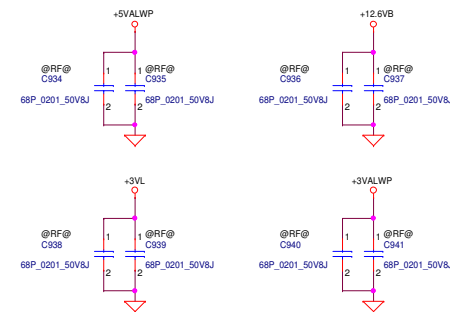
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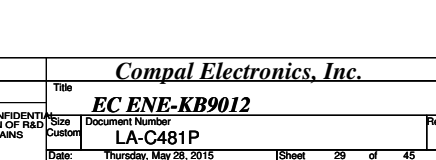
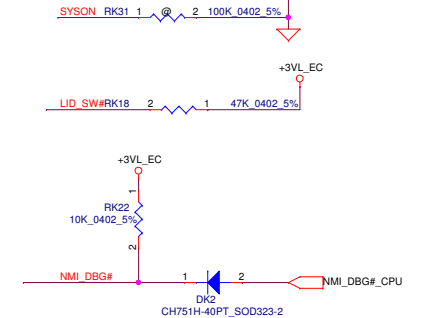
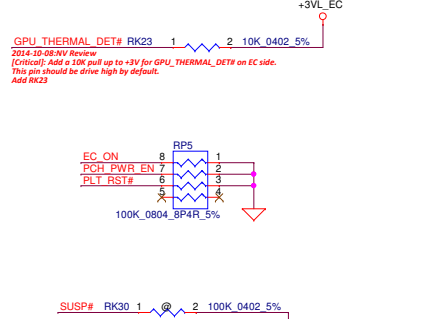
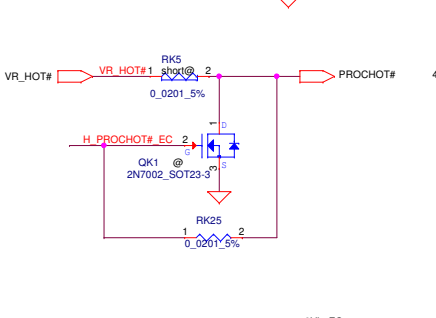
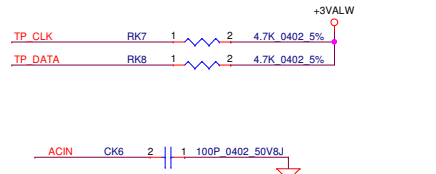
Screw Hole



RF Reserve

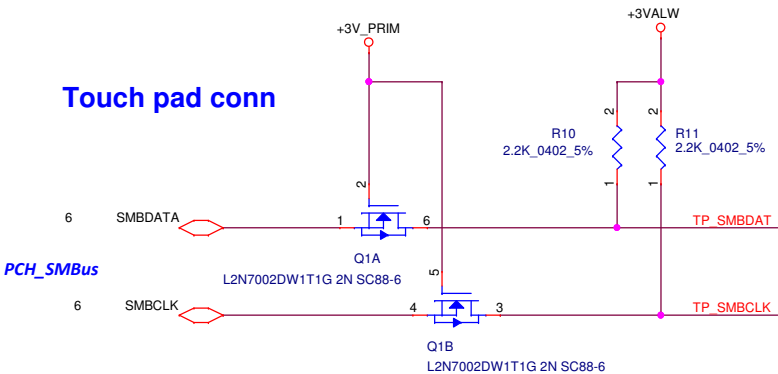


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				TPM/G-SENSOR/13"Screw hole	
				Size	Document Number
				LA-C482P	
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		Rev	0.3		



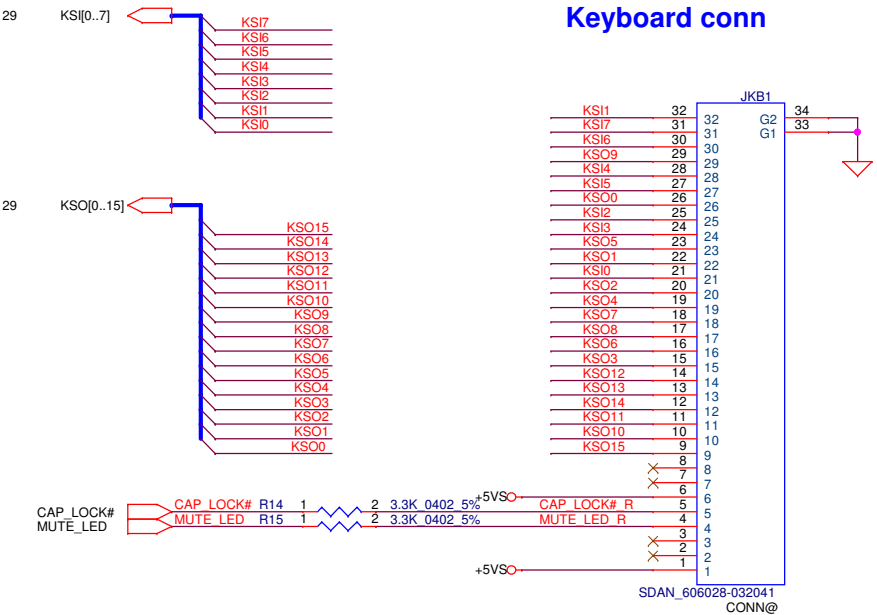
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title		
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Touch pad conn

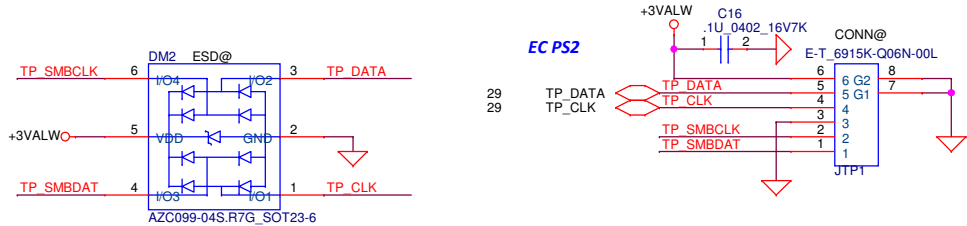


PCH_SMBus

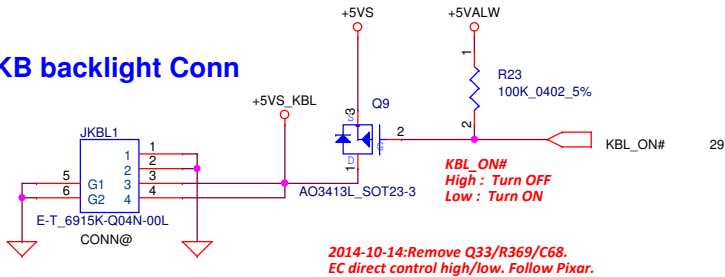
Keyboard conn



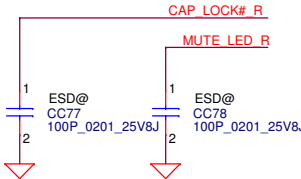
EC PS2



KB backlight Conn

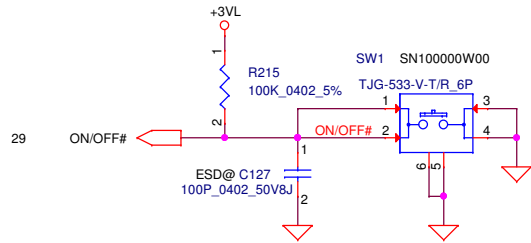


2014-10-14: Remove Q33/R369/C68.
EC direct control high/low. Follow Pixar.

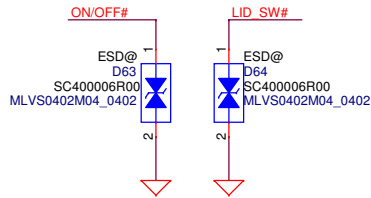


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Size B		Document Number		Rev	
Date:		Thursday, May 28, 2015		Sheet 30 of 45	
				LA-C482P	
				0.3	

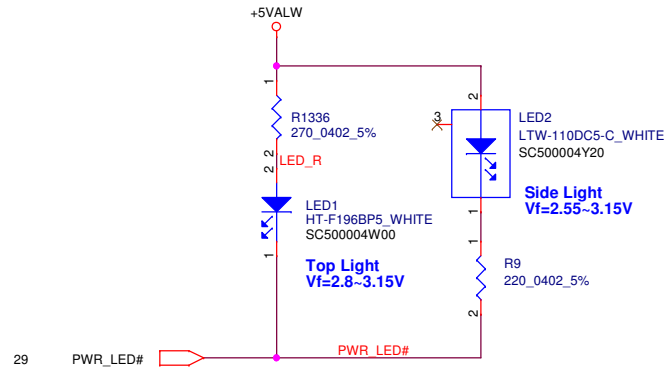
Power Button Switch



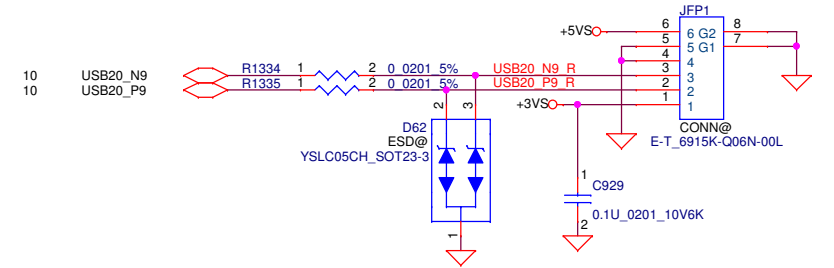
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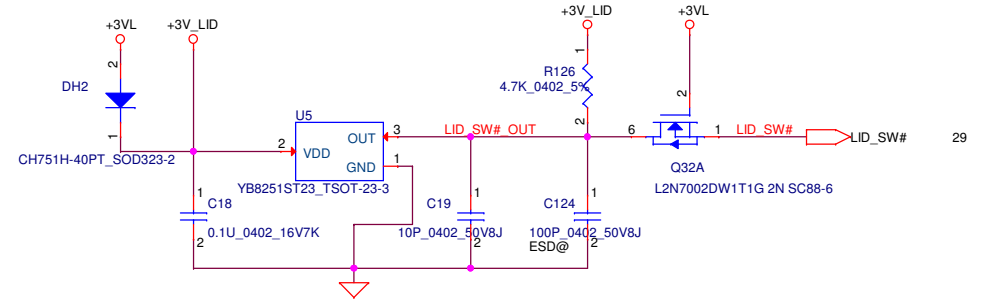
Power ON LED



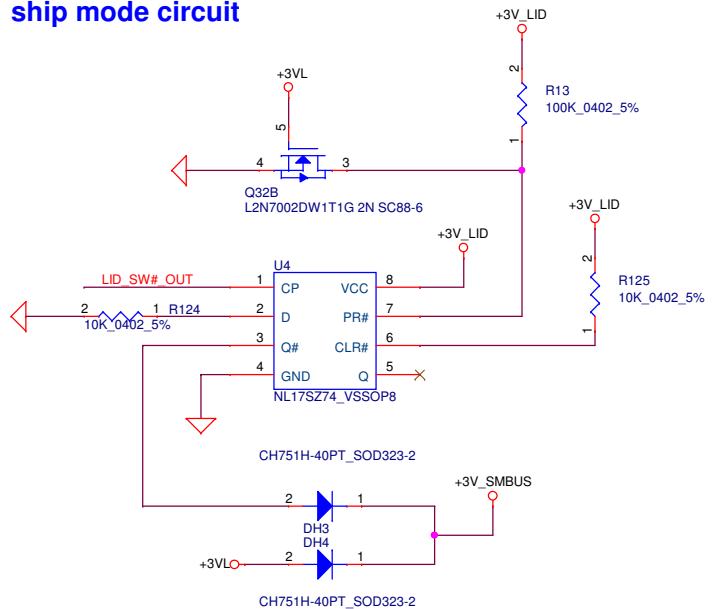
Finger printer



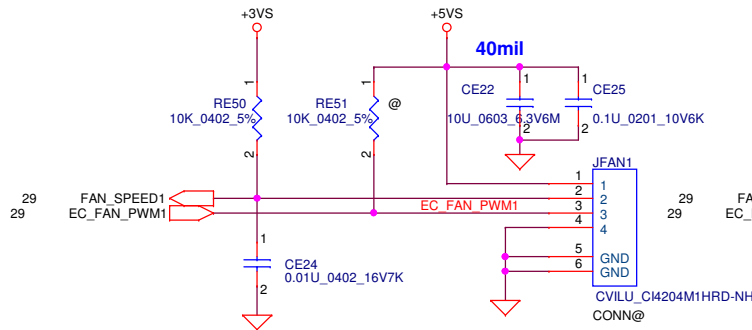
Lid Switch (Hall Effect Sensor)



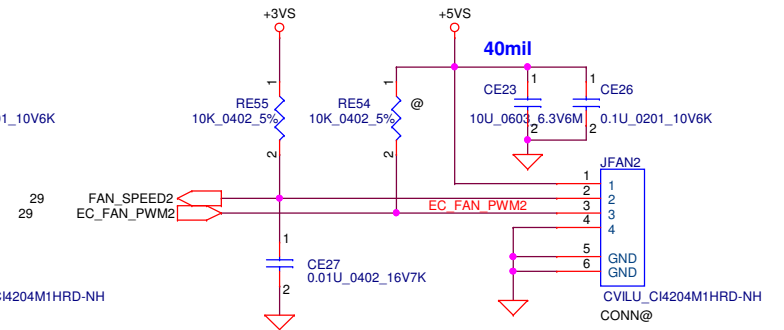
ship mode circuit



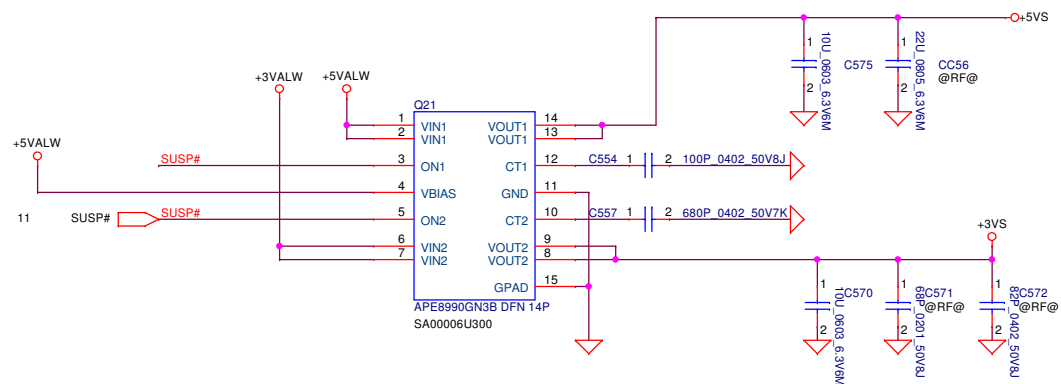
FAN Conn1



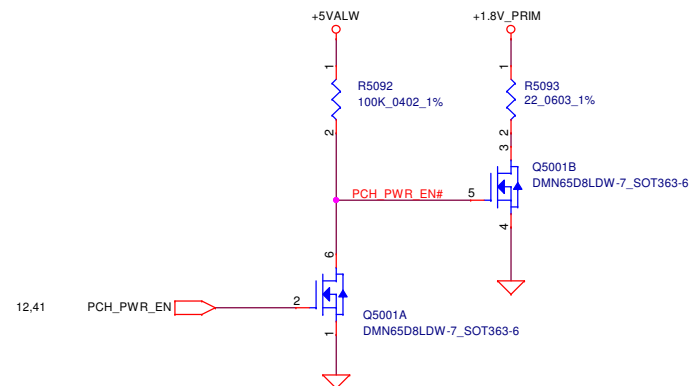
FAN Conn2



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For +1.8V_PRIM Discharge



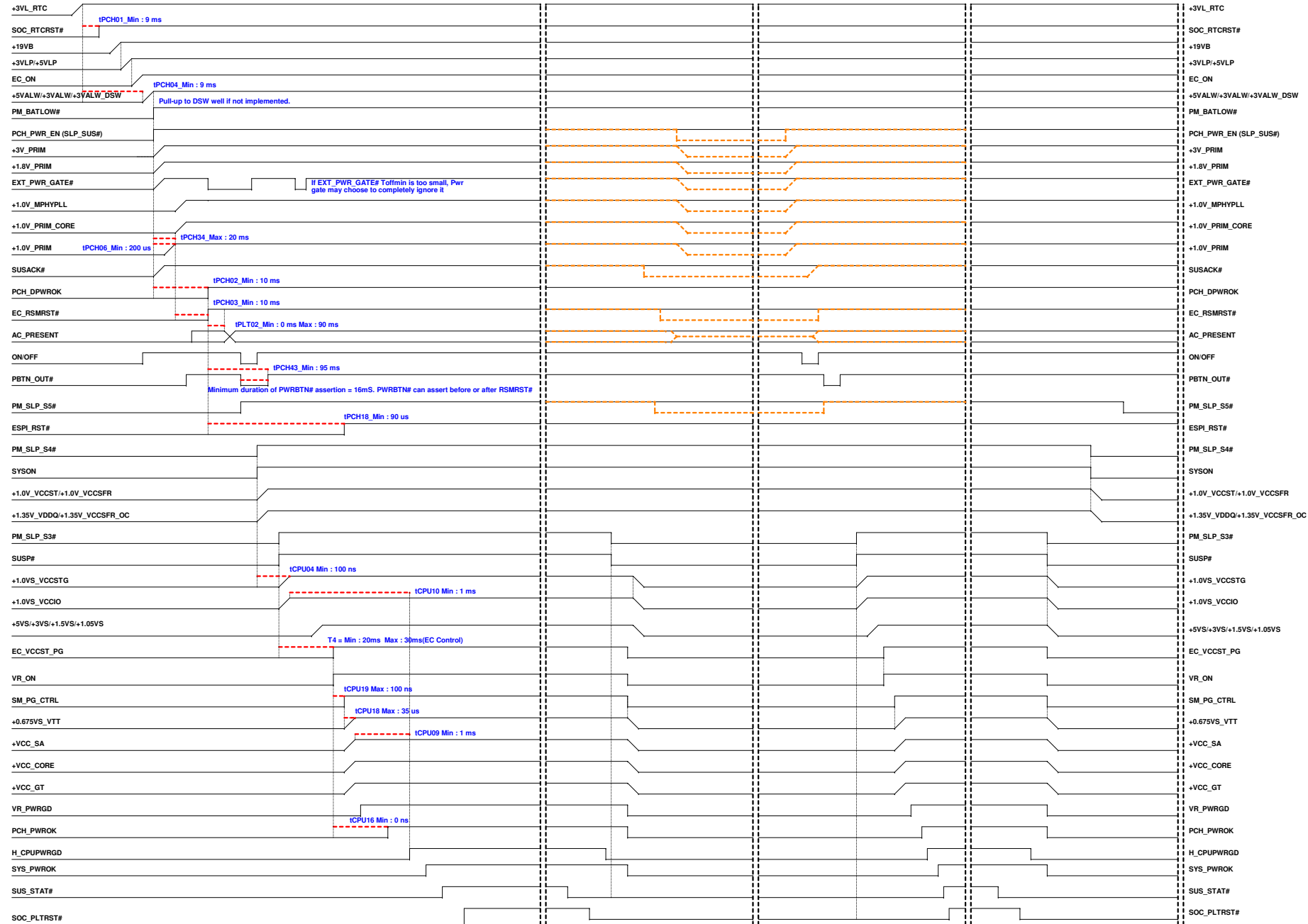
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Issued Date	2011/06/29	Deciphered Date	2011/06/29	Title	
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Size	Custom	Document Number	LA-C482P	Rev	0.3
Date:	Thursday, May 28, 2015	Sheet	32	of	45

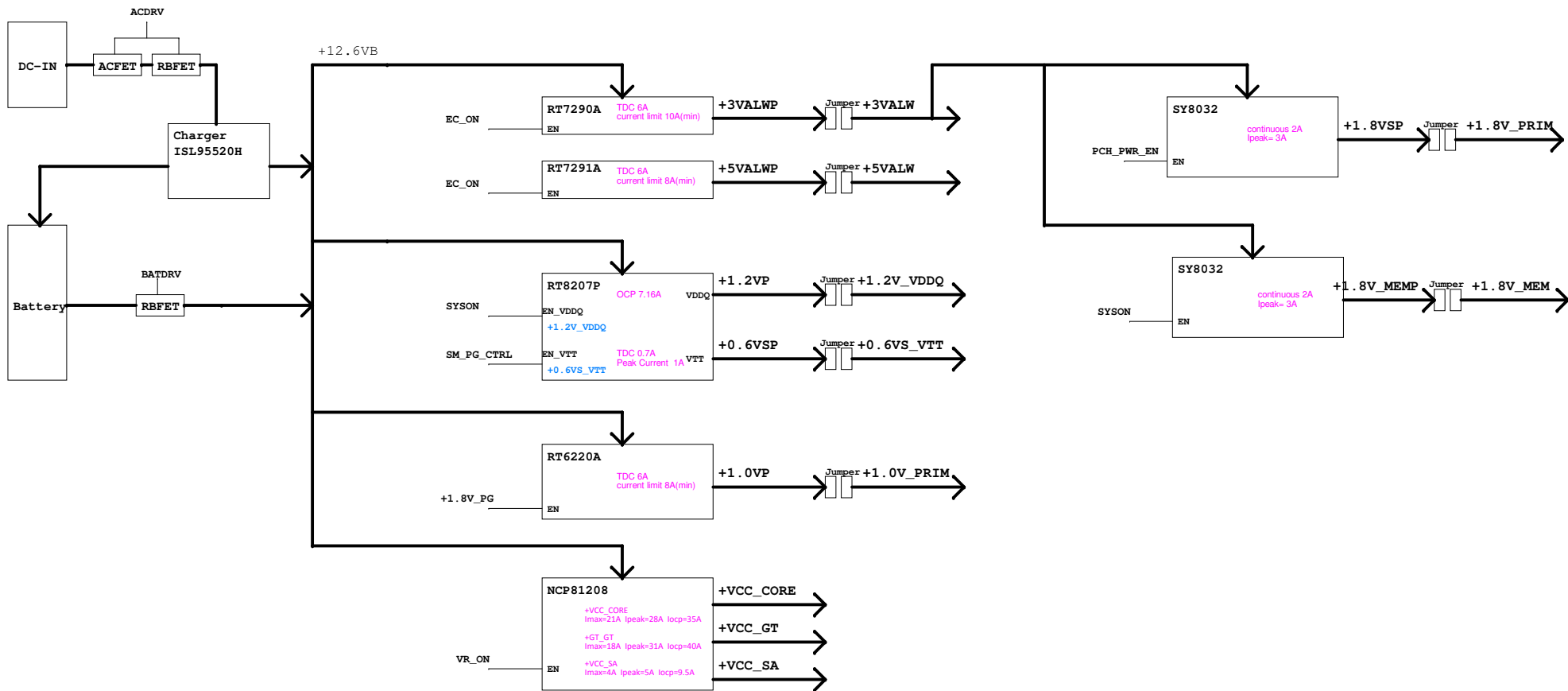
G3→S0

S0→S3/DS3

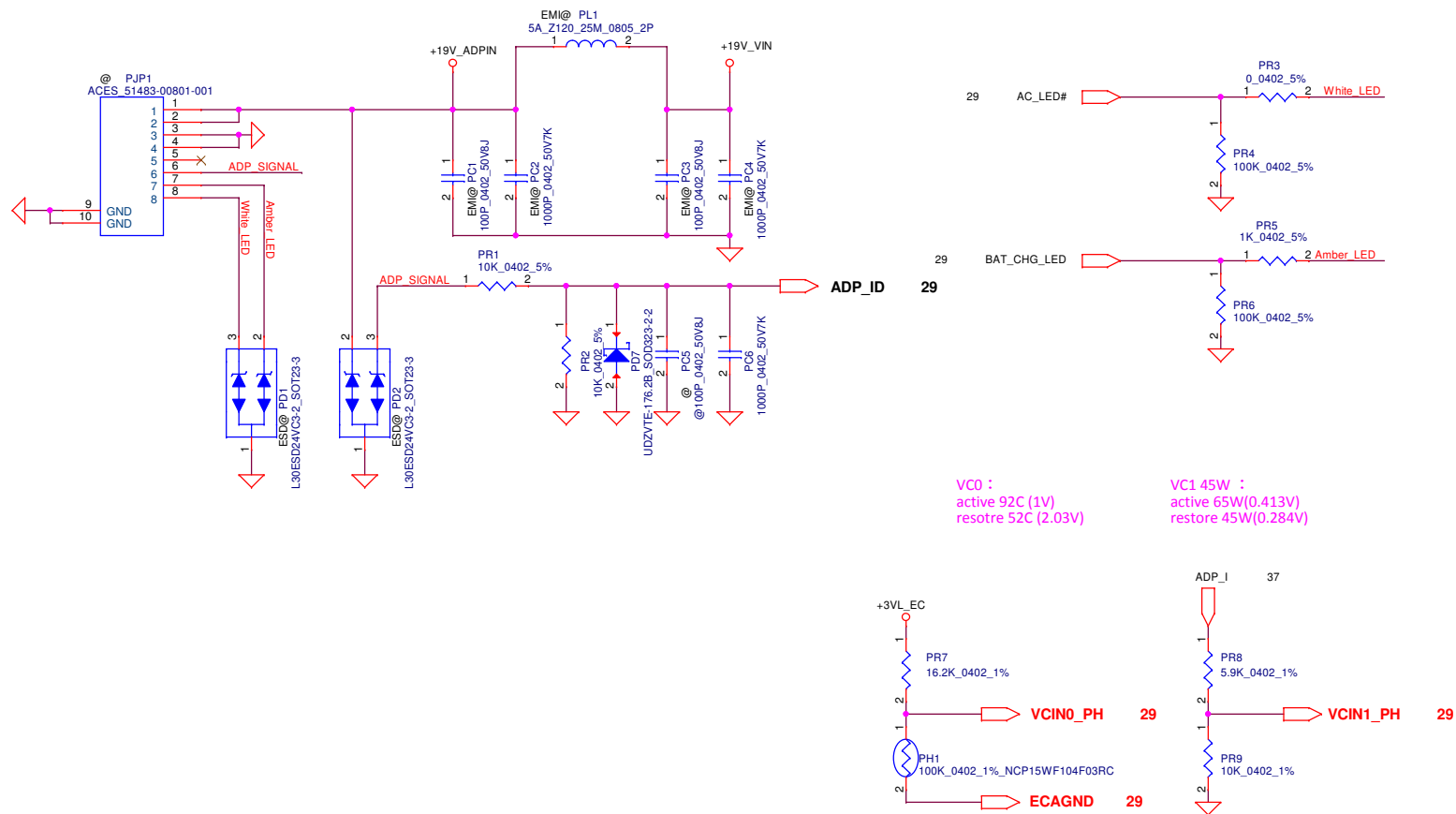
S0/DS3→S0

S0→S5

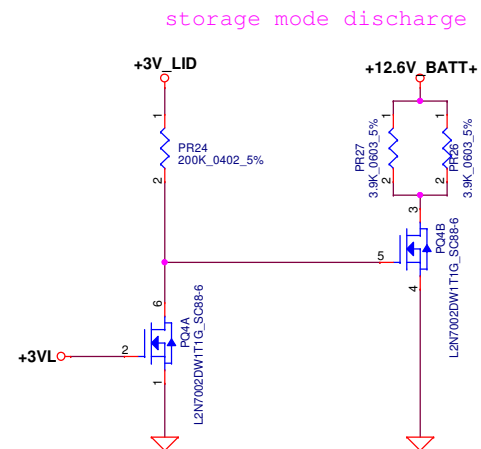
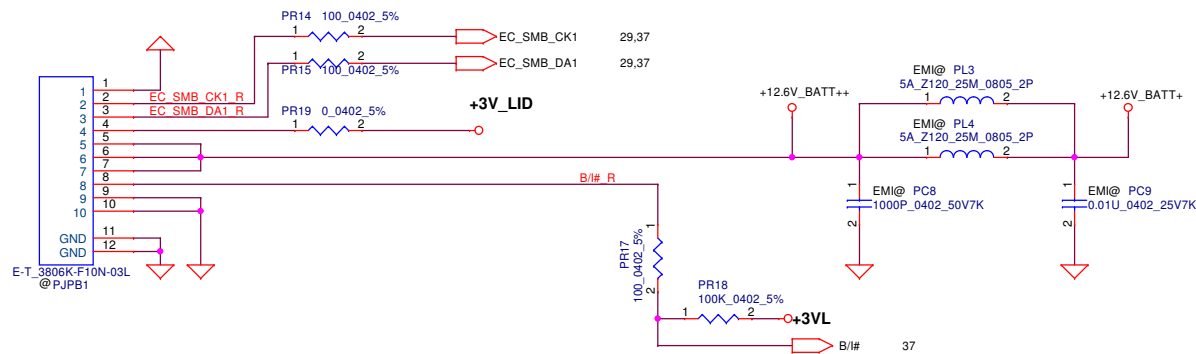




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Size	Document Number			Rev	
	LA-C482P			0.1	
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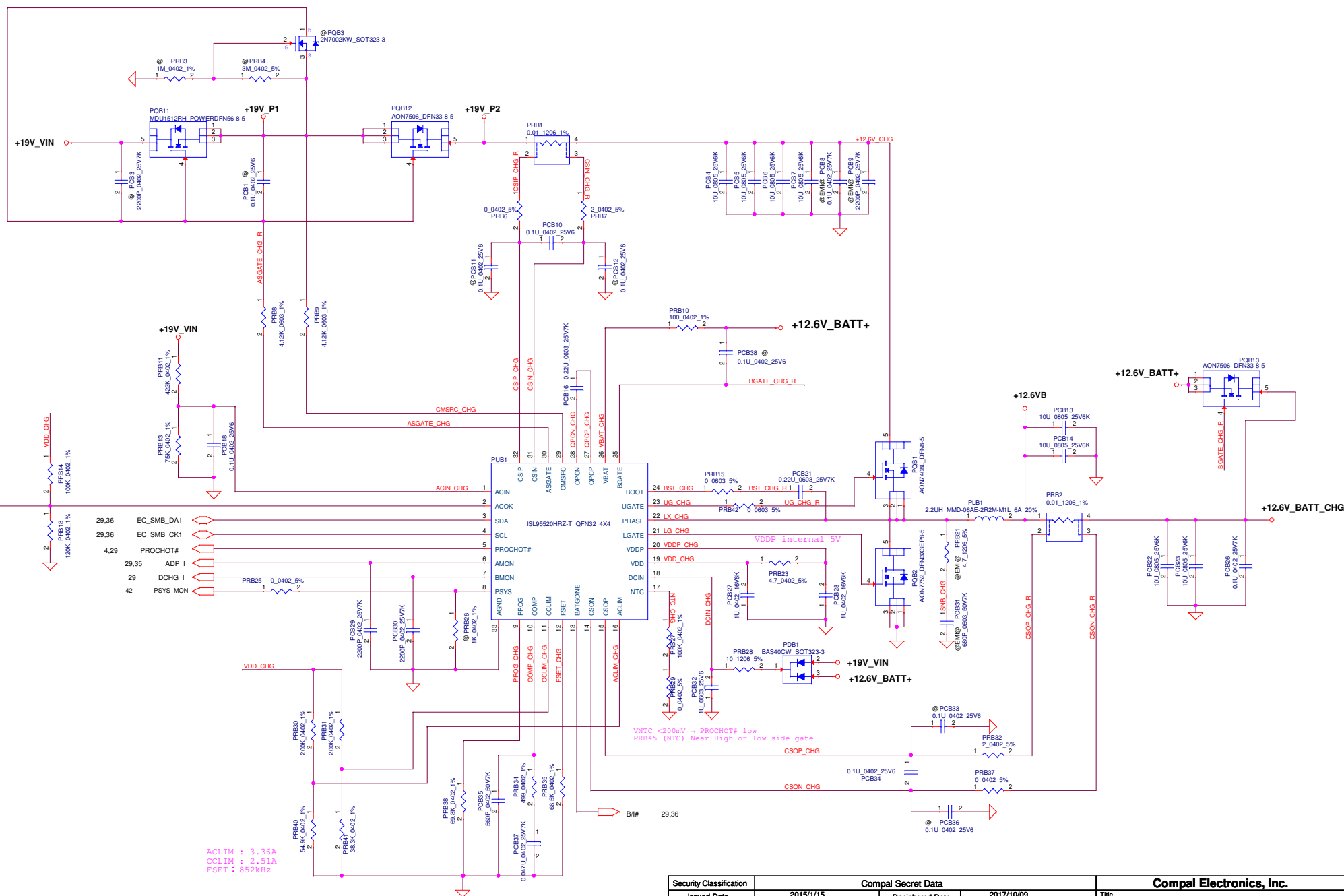


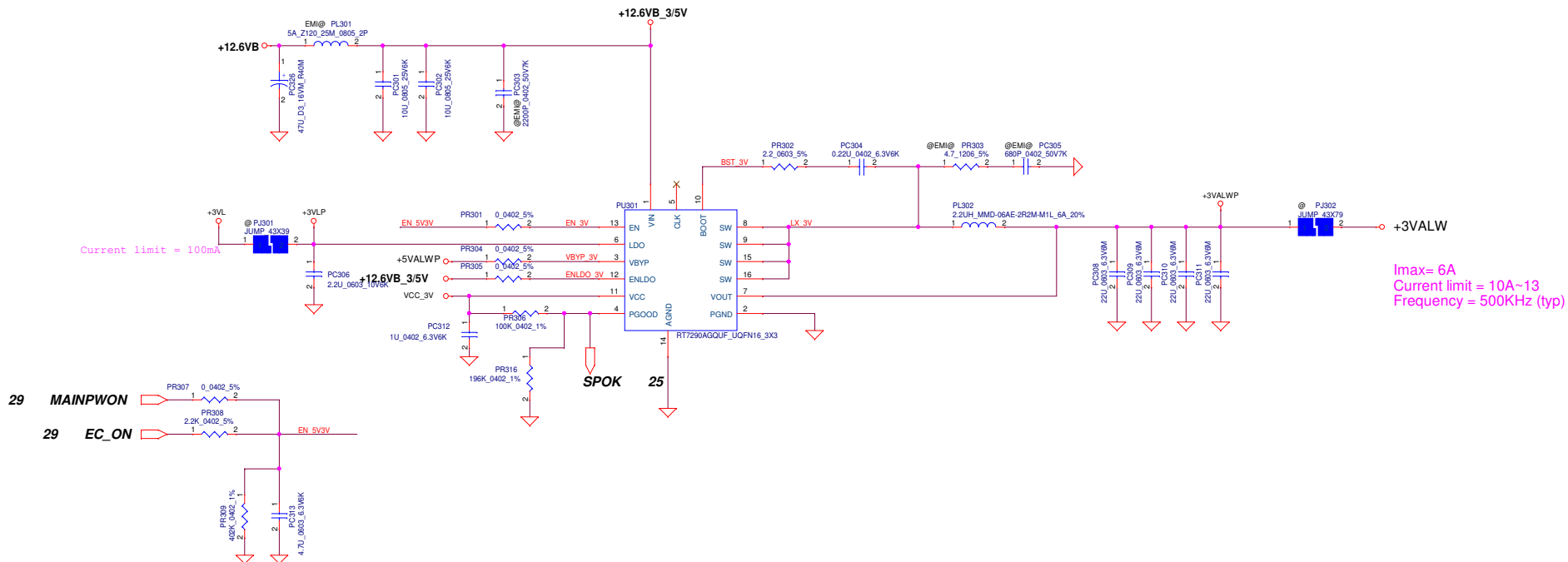
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/1/15	Deciphered Date	2017/10/09	Title DC Conn	
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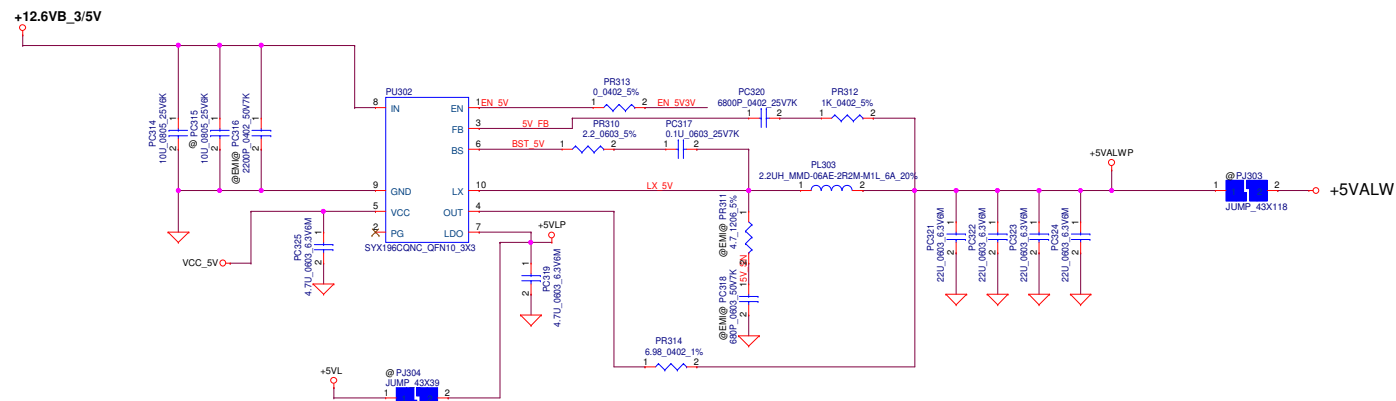
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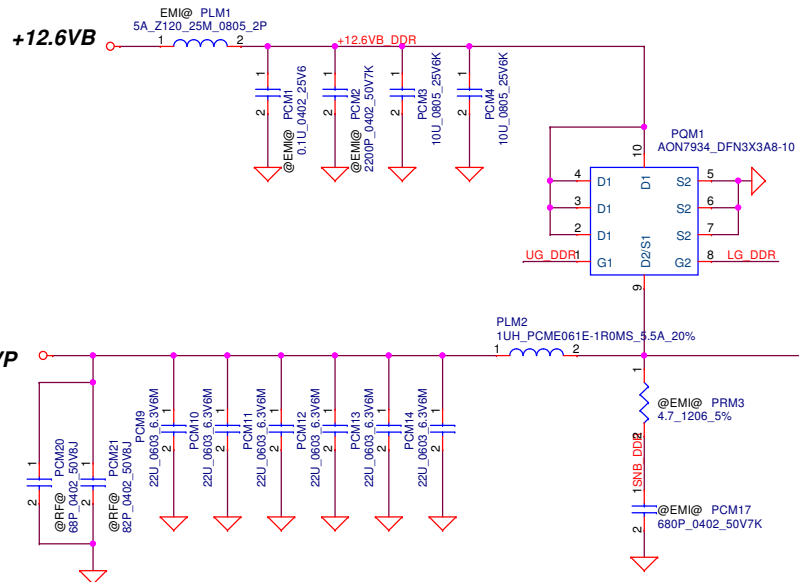


29 MAINPWON

29 EC_ON



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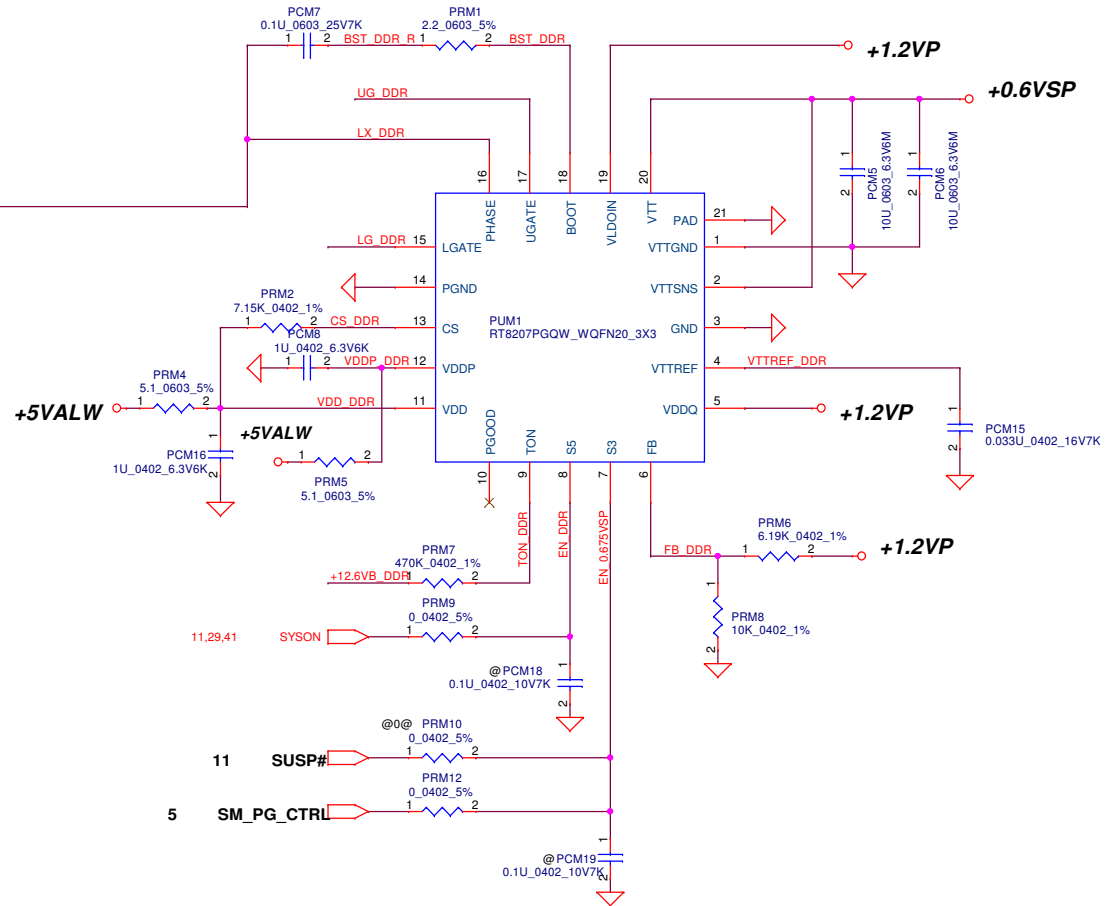


+1.2VP @PJM1
JUMP_43X118

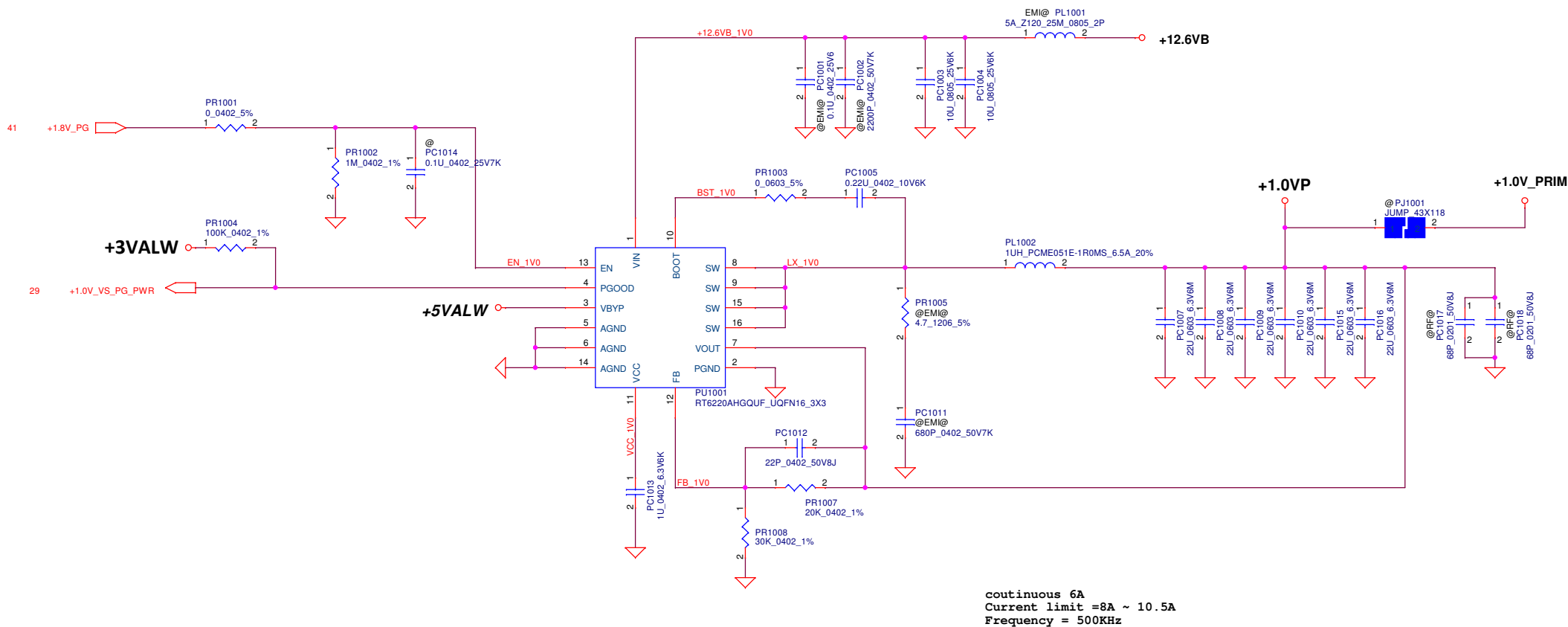
+0.6VSP @PJM2
JUMP_43X39

Switching Frequency:540kHz
I_ocp : 7.16A
OVP : 113%~120%

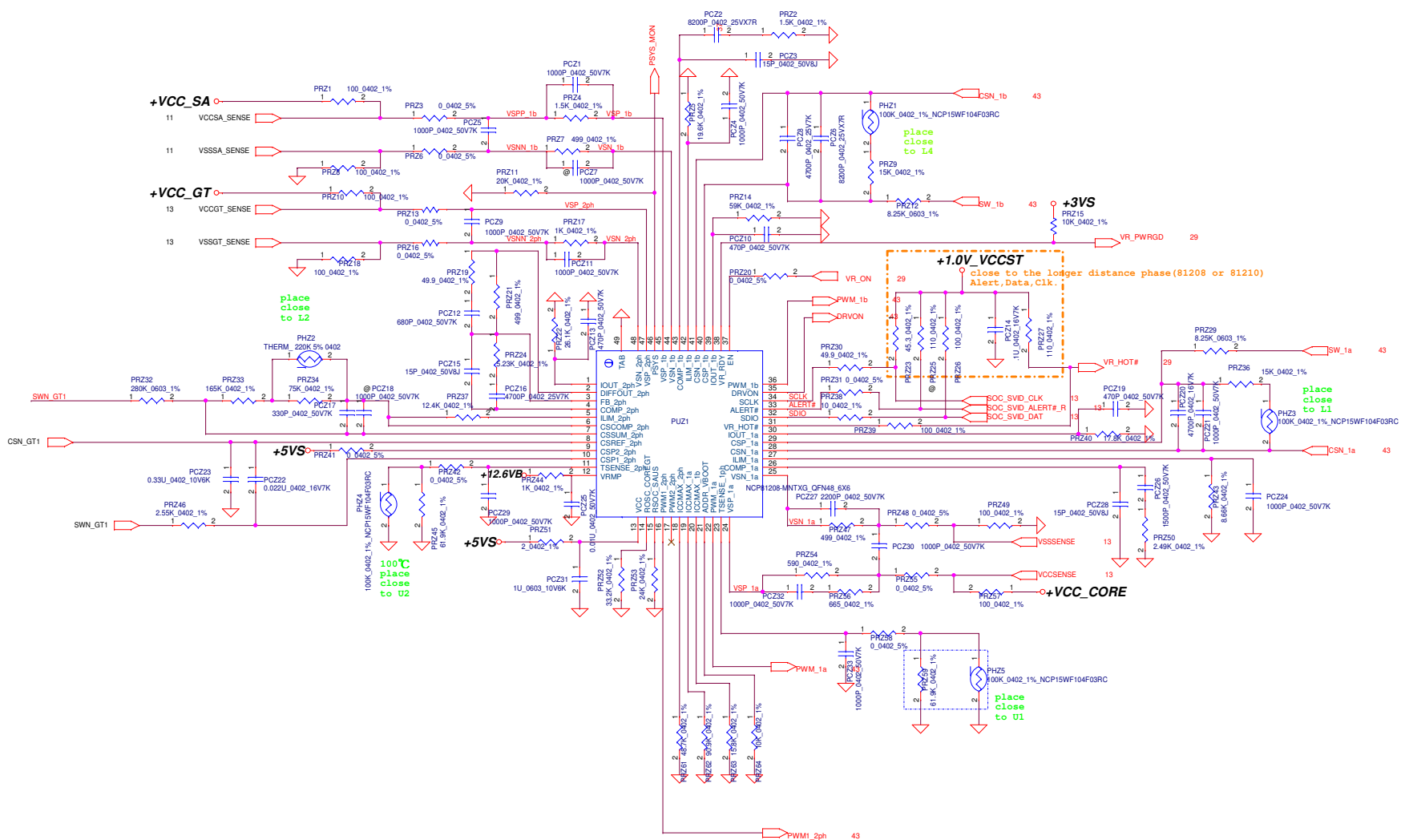
+0.6VS_VTT
TDC 0.7A
Peak Current 1A

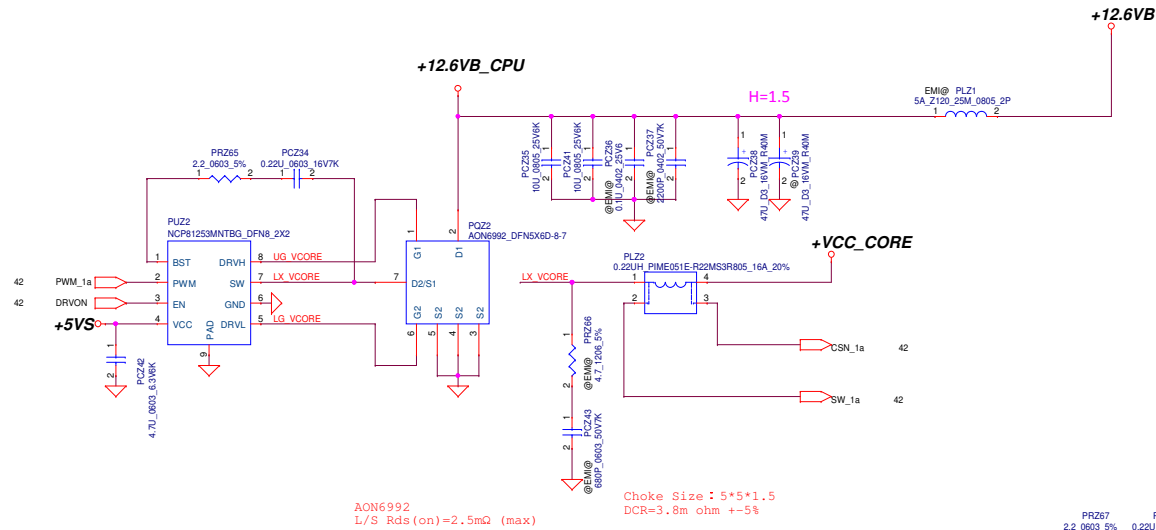


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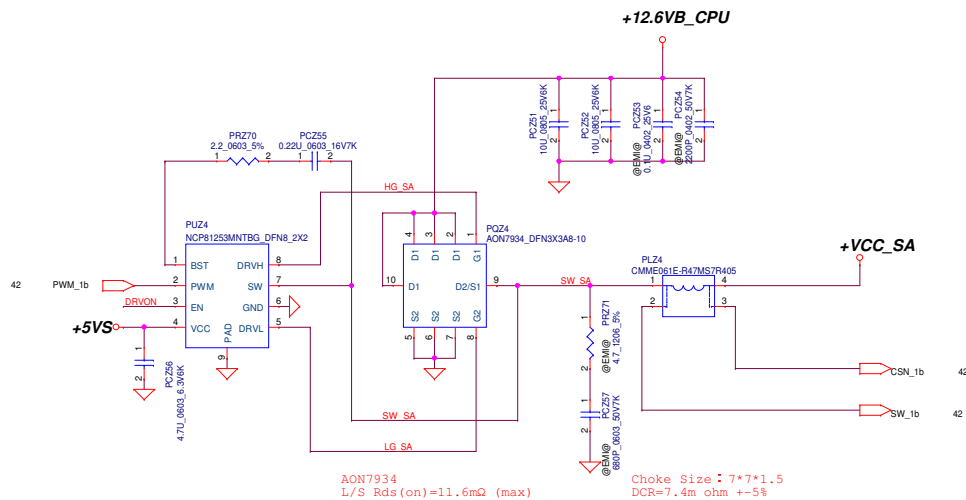
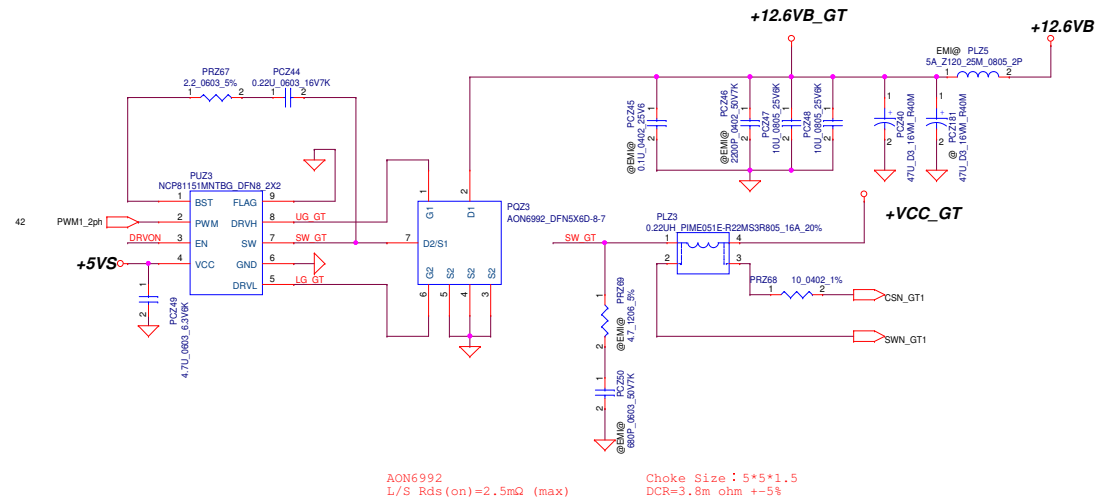




IA
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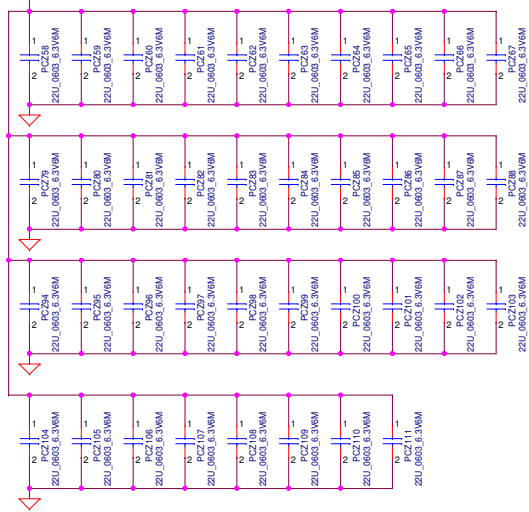
GT
Imax=18A Ipeak=31A Iocp=40A

VCCSA
Imax=4A Ipeak=5A Iocp=9.5A

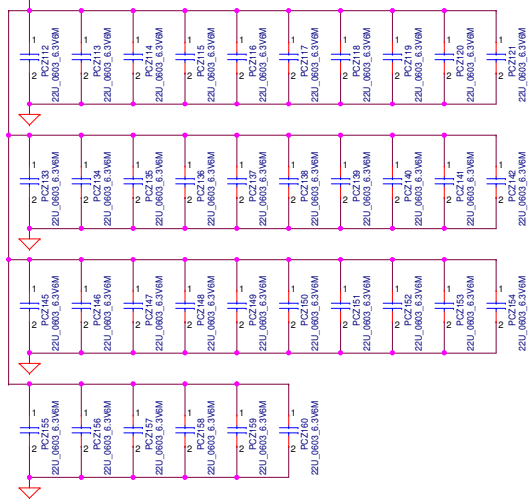


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Size	Document Number	LA-C482P			Rev
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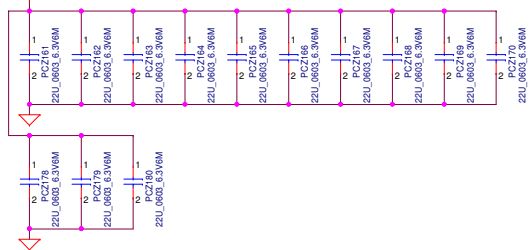
+VCC_CORE



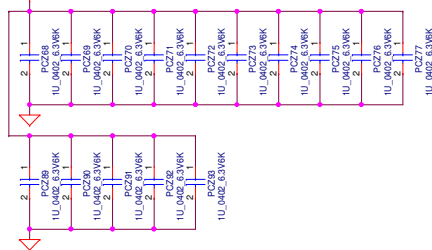
+VCC_GT



+VCC_SA



+VCC_CORE



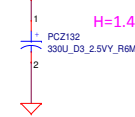
VCC Output Cap :
22U 6.3V X5R 0603 * 38
1U 6.3V X5R 0402 * 15
330U 2.5V D2 ESR6M * 1

+VCC_CORE



H=1.4

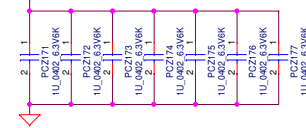
+VCC_GT



H=1.4

VCCGT Output Cap :
22U 6.3V X5R 0603 * 36
1U 6.3V X5R 0402 * 12
330U 2.5V D2 ESR6M * 1

+VCC_SA



VCCGT Output Cap :
22U 6.3V X5R 0603 * 13
1U 6.3V X5R 0402 * 7

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Size	Document Number	LA-C482P			Rev
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